ADDENDUM

MODEL 859-S-902
50 MH PROGRAMMABLE
PULSE GENERATOR

WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

ADDENDUM

MODEL 859-S-902
50 MH PROGRAMMABLE
PULSE GENERATOR

This addendum amends *Instruction Manual, Model 859* (Dated 3/84) for use with the Model 859-S-902.

© 1984 Wavetek

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO WAVETEK AND IS SOLELY FOR INSTRUMENT OPERATION AND MAINTENANCE. THE INFORMATION IN THIS DOCUMENT MAY NOT BE DUPLICATED IN ANY MANNER WITHOUT THE PRIOR APPROVAL IN WRITING FROM WAVETEK.

WAVETEK®

WAVETEK SAN DIEGO, INC.
9045 Balboa Ave., San Diego, CA 92123
P. O. Box 85265, San Diego, CA 92138
Tel 619/279-2200 TWX 910/335-2007

Addendum Date: 12/84

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_09850

FOREWORD

IMPORTANT

The information in this addendum replaces or amends portions of the Model 859 Instruction Manual (Dated 3/84). Where no changes are indicated, those portions of the manual are applicable with this stipulation:

1. *Disregard references to the keyboard and display for normal (GPIB) operation.*
2. *Disregard references to stored settings, vernier control and to the second channel being optional.*

This addendum describes the difference between the standard Model 859 and the Model 859-S-902. Major differences are:

1. *Front Panel:* The standard 859 front panel has been replaced with a flat panel. There is no keyboard or display. There is a power switch and a power ON indicator. All front panel descriptions in the standard manual are not applicable.

2. *Second Output Channel:* The 859-S-902 includes a second output channel identical to the standard channel. This is the optional channel discussed in the standard manual.

3. *Stored Settings:* The 859-S-902 has no stored settings. All stored settings descriptions in the standard manual are not applicable.

4. *Sync Output and Clock Output:* The standard 859 SYNC OUT and CLOCK OUT output levels have been modified to be ECL compatible. When the output is loaded with a 50 ohm terminator, output levels are switching between 0 and -800 mV typically.

5. *Trigger Input:* The 859-S-902 trigger threshold level is preset to -400 mV and TRIGGER LEVEL adjust on the rear panel is removed.

6. *Maximum Delay:* The maximum pulse delay has been modified to 1599 ms instead of 999 ms.

7. *Specifications:* Model 859 specifications do not apply. General Dynamics Drawing No. 3202267 is the basis for the specifications included in this addendum.

8. *Drawings:* Selected assembly drawings, schematics and parts lists in the Model 859 manual are superceded by this addendum.

9. *Operation:* There are two ways to operate the Model 859-S-902:
   a. The Model 859-S-902 has no keyboard or display. Normally, instrument settings must be programmed via the General Purpose Interface Bus (GPIB) interface. Refer to this addendum for GPIB-only use.
   b. For instrument maintenance, a cable-connected front panel with keyboard and display is available. Refer to the standard manual for instrument use with keyboard and display.

CONTENTS

SECTION 1 CHANGES

1.2 Minimum Specificatons 1-1
1.3 Full Specifications 1-1

SECTION 2 CHANGES

2.2.2 Signal Connections 2-1
Table 2-3. Initial Checkout 2-2
Table 2-4. Acceptance Test Record 2-5
Table 2-5. Performance Checkout 2-6
Table 2-6. Performance Test Record 2-14

SECTION 3 CHANGES

3.8.3 Delay 3-1
3.9.6 Sync Output 3-1
3.9.7 Clock Output 3-1
3.11.4 Talker 3-1
3.11.7 GET Mode 3-1

SECTION 4 CHANGES

4.3 Delay and Width One Shots 4-1
4.6 Trigger Comparator 4-1
4.13 Clock Output 4-1
4.14 Sync Output 4-1

SECTION 5 CHANGES

5.9 Removal and Installation Procedures 5-1
Table 5-12. Control Bit Code Definition 5-22

SECTION 7 CHANGES

List of Assembly Drawings, Parts Lists and Schematics 7-1

Model 859-S-902

SECTION 1
GENERAL DESCRIPTION

1.2 MINIMUM SPECIFICATIONS

1.2.1 Repetition Rate

Programmable: 0.5 Hz to 10 MHz.
Resolution: 3 digits of programmed value.

1.2.2 Pulse Width

Programmable: 20 ns to 100 ms.
Resolution: 20 ns for 20 ns ≤PW <10 μs, 500 ns for 10 μs ≤PW <100 μs, 1 μs for 100 μs ≤PW <1 ms, 1 ms for 1 ms ≤PW ≤100 ms.

1.2.3 Delay

Programmable: 0 to 1.599 s.
Resolution: 20 ns for 20 ns ≤Delay <10 μs, 1 μs for 10 μs ≤Delay <1 ms, 100 μs for 1 ms <100 ms, 1 ms for 100 ms ≤Delay <1.6 s.

1.2.4 Rise/Fall Time

Programmable: 5 ns to 500 ns.
Resolution: 5 ns for 5 ns ≤R/F <50 ns, 10 ns for 50 ns ≤R/F <200 ns, 20 ns for 200 ns ≤R/F <500 ns.
Over/Undershoot: 5% of p-p amplitude ±10 mV into 50Ω.

1.2.5 Pulse Amplitude Requirements

Voltage Range Programmable: −15 to +15 V, with baseline at 0 V.
Minimum Pulse Amplitude and Resolution: 50 mV.
Voltage Accuracy: 3% program value ±1% p-p amplitude ±100 mV.
Drive Capability: Programmable voltage outputs shall provide sufficient drive capability to meet amplitude requirements under the following conditions:

1. Single ended driver, dc isolated from chassis, impedance 1 MΩ.
2. Single ended driver, dc isolated from chassis, impedance 50 Ω.

Dual Channels: All parameters, except frequency, are independently controlled.

1.2.6 General

Operating Temperature: 0° to 50°C.
Temp. for Spec. Operation: 20° to 45°C.
Warm-up Time: 30 minutes.
Altitude: Sea level to 10,000 ft.
Relative Humidity: 80% non-condensing.
Weight: 70 pounds.
Power: 90 to 250 Vrms, 48 to 67 Hz, 250 VA.

1.3 FULL SPECIFICATIONS

1.3.1 Versatility

1.3.1.1 Pulse Outputs

There are four pulse outputs.

1. Two channels of variable pulses. Channels share operating mode and internal clock period only; all other functions and parameters are independent.
2. Sync pulse and clock pulse which are fully compatible with the 10192 ECL driver; will drive a 10514 receiver when output is terminated with 50Ω load. Sync pulse is at lowest frequency in generator system. Clock is a 50% duty cycle pulse with programmable repetition rate (see paragraph 1.3.2.3).

1.3.1.2 Operational Modes

Continuous: Output continuous at programmed frequency.

Triggered: Output quiescent until triggered for one single or double pulse.

Gated: As triggered mode, except repetition rate generator is enabled for duration of input trigger. Last pulse period started is completed. Maximum gate rate is 5 MHz.

Burst: As triggered mode, except repetition rate generator is enabled for programmed number of pulse periods from 1 to 10,000.

External Width: Trigger duration and rate set pulse width and repetition rate.

Time Interval: Trigger causes one pulse with programmed width: 20 ns to 9999s.

Resolution: To nearest 20 ns for width <100 μs. To 4 digits for width ≥100 μs.

Duty Cycle: 90% limited by 100 ns off time.

1.3.1.3 Pulse Functions

Single: One pulse each pulse period. Up to 10 MHz repetition rate.

Double: one pair of pulses each pulse period. Up to 5 MHz repetition rate. Both pulses have programmed width. Position of second pulse set by delay control.

Square: Pulse is fixed symmetrical (50% duty cycle) up to 10 MHz repetition rate with variable transition times to 5 ns.

Inhibit: Disconnected output and no error checking on channel.

1.3.2 Pulse Outputs

1.3.2.1 Main Output

Upper and lower pulse levels of both main output channels are independently programmable. High impedance or 50Ω source impedance automatically selected. If upper level, lower level or peak-to-peak amplitude is >|10V|, the 50Ω internal source is changed to high impedance. The values in table 1-1 are for 50Ω load impedance.

Pulses of either output channel may be normal or complement. In complement, upper and lower levels are interchanged. Transition times remain as programmed.

Table 1-1. Pulse Output Specifications

Characteristics	High Impedance Source	50Ω Source
Upper Level Range	−12.00 to ±20.00V	−9.96 to +10.00V
Lower Level Range	−20.00 to +12.00V	−10.0 to +9.96V
Resolution (digits of programmed value)	<3 digits (20 mV)	3 digits (10 mV)
Amplitude	8.00 to 20.00V	40 mV to 10V
Accuracy	3% program value ±1% ampl ±100 mV	3% program value ±1% ampl ±50 mV
Repeatability	Highly dependent upon cable length and load impedance	±1% ampl ±50 mV
Preshoot		±3% ampl ±10 mV
Overshoot and Ringing		±3% ampl ±10 mV

1.3.2.2 Sync Output

A pulse at lowest frequency in generator system.

1.3.2.3 Clock Output

A pulse of 50% duty cycle and with programmed repetition rate in continuous, gated and burst modes. repetition rate in time inverval mode determined by microprocessor.

1.3.3 Time Domain

1.3.3.1 Repetition Rate

Frequency Range: 0.5 Hz to 10 MHz.

Period Range: 100 ns to 2s

Resolution: 3 digits of programmed value.

Jitter: 0.1% ±50 ps.

1.3.3.2 Width

Width control affects pulses of the main channels.

Range: 10 ns to 999 ms.

Resolution: 1 ns from 10 ns to 19.999 μs; 3 digits of programmed value from 20 μs to 999 ms.

Jitter: ±0.1% ±50 ps width <1 μs; ±0.05% width 1 to 10 μs; ±0.005% width >10 μs.

Duty Cycle: 90% limited by 10 ns minimum off time.

1.3.3.3 Delay

Delay control affects pulses of the main chassis.

Range: 0 ns to 1599 ms.

Resolution: 1 ns from 0 ns to 19.999 μs; 3 digits of programmed value from 20 μs to 999 ms.

Jitter: ±0.1% ±50 ps delay <1 μs; ±0.05% delay 1 to 10 μs; ±0.005% delay >10 μs.

Duty Cycle: 90% limited by 10 ns minimum off time for delay <25 ns and by 20 ns minimum off time for delay ≥25 ns.

1.3.3.4 Transition Time

For pulses of either main channel, leading and trailing edge transition time adjustable from .5 ns to 25 ms (10% to 90% points of programmed amplitude).

Transition Times: Variable to 50:1.

Leading and trailing edge times must be in the same range:

5 ns to 100 ns;
50 ns to 2.5 μs;
500 ns to 25 μs;
5 μs to 250 μs;
50 μs to 2.5 ms;
500 μs to 25 ms.

Resolution: 3 digits of programmed value when both transitions are in the first 10:1 portion of their transition time range, decreasing to 2 digits at 50:1.

Linearity: ±3% for transitions >50 ns.

1.3.3.5 Typical System Delays

Fixed trigger input to sync output delays for each mode.

Triggered: 60 ±10 ns.
Gated: 100 ±10 ns.
Burst: 100 ±10 ns.
External Width: 40 ±10 ns.
Time Interval: 80 ±10 ns.

1.3.4 Input Characteristics

1.3.4.1 External Trigger

Rising or falling edge triggering selectable.
Trigger Level: Compatible with the 10514 receiver.
Input Impedance: 50Ω.

1.3.4.2 GPIB Trigger

ASCII **J**. In gated and external width modes, **H** signals end of active interval.

1.3.4.3 GPIB

IEEE 488-1978 compatible for direct connection to GPIB. Optical isolation. Capabilities are as follows.

Listener: AH1 and L4.
Talker: SH1 and T6.
Service Request: SR1.
Remote Local: RL1.
Device Clear: DC1.
Device Trigger: DT1.
Table 1-2 shows typical programming times.

1.3.5 General

1.3.5.1 Environmental

Specifications apply for 20° to 45°C after 30 minutes warm-up. Burn-in temperature 50°C for 96 hr maximum. Instrument will operate from 0 to 50°C, 0 to 10,000 feet and from 0 to 95% relative humidity at 25°C.

1.3.5.2 Dimensions

Fits standard 48.3 cm (19 in.) rack. Dimensions behind front panel are 43.2 cm (17 in.) wide; 13.3 cm (5¼ in.) high; 58.4 cm (23 in.) deep. Supplied with rack mount adapters.

Table 1-2. Typical Programming Time

Parameter	Time
Command Handshake	2 μs
Data Handshake	220 μs
Frequency	15 ms
Period	20 ms
Upper Level	20 ms
Lower Level	20 ms
Delay	15 ms
Width	18 ms
Leading	35 ms
Trailing Edge	35 ms
Time Interval	10 ms
Mode	10 ms
Function	5 ms
Channel	7 ms
Trigger Format	5 ms
Normal/Complement	5 ms
Output ON/OFF	5 ms
Burst Number	8 ms
Trigger	3 ms
Execute	20 ms*
GET	2 ms

*2.5 ms when via GET.

NOTE: Preceeding programming times are typical and may vary with different controllers.

1.3.5.3 Weight

26.3 kg (58 lb) net; 32 kg (70 lb) shipping.

1.3.5.4 Power

90 to 105V, 108 to 128V, 198 to 321V or 216 to 252V; 48 to 66 Hz. Power consumption 250 VA.

NOTE

Specifications apply with transition time set to minimum; with a 50Ω source driving a 50Ω load.

SECTION 2
INSTALLATION AND INTERFACE

2.2.2 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

TRIG IN: ECL compatible, 50Ω impedance.

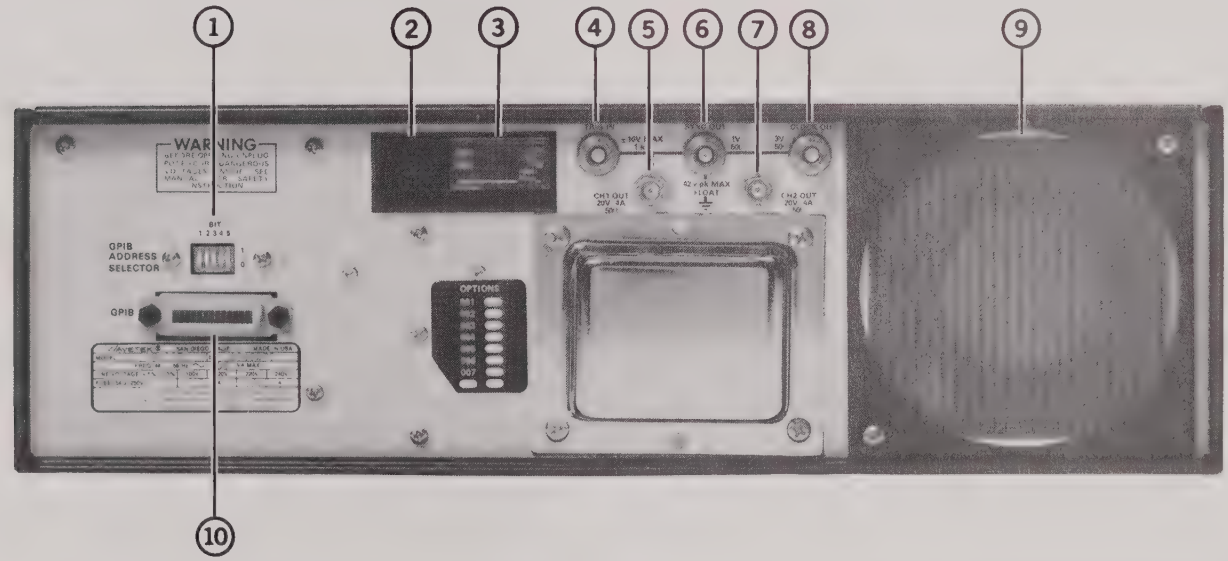
SYNC OUT: ECL compatible.

CLOCK OUT: ECL compatible.

CH1 OUT: 20V into 50Ω load.

CH2 OUT: 20V into 50Ω load.

BNC ground may be floated a maximum of 42V peak.



Location	Function	Paragraph
1	GPIB address selector DIP switch	2.2.4
2	Power cord receptacle	2.2.1
3	Fuse and fuse holder	2.2.1
4	Trigger signal input BNC	2.2.2, 3.7.2
5	Channel 1 output BNC	2.2.2, 3.9
6	Sync output BNC	2.2.2, 3.9.6
7	Channel 2 output BNC	2.2.2, 3.9
8	Clock output BNC	2.2.2, 3.9.7
9	Air filter screen	
10	GPIB connector	2.2.3

Figure 2-2. Rear Panel and Cross Reference

Table 2-3. Initial Checkout

Step	Test	Tester & Setup	Program	Desired Results
1	Self Test	None	Power: ON	859 displays *SELF-TEST* for less than 5s, then *WAVETEK 859*
2	Wake-Up State	Connect 859, oscilloscope and trigger source as in figure 2-3. Scope settings: CH1 0.5 V/Div CH2 0.5 V/Div Horizontal 0.2 ms/Div External trigger	Output: P1I	Scope: 1 kHz, 1 Vp-p square wave
3	CH1 Output Levels	Scope setting: CH1, 5 V/Div	Upper Level: A5I	Scope: Level increases positively to 5 V
4			Lower Level: D-5I	Scope: Level increases negatively to −5V
5			Reprogram levels: A10D0I	Scope: 10V upper level, 0V lower level square wave
6	CH1 Normal/Complement Output		Width: N3E-4 Function: C0I	Scope: 1 kHz pulse.
7			Complement Output: O1I	Scope: Complement of previous pulse.
8			Output: O0I	Scope: Pulse width increases.
9	CH1 Width		Width: N1E-6I	Scope: Pulse width 1 μs.
10			Width: N20E-6I	Scope: 20 μs wide pulse.
11	CH1 Delay		Delay: L1E-6I	Scope: Pulse delay 1 μs.
12	CH1 Leading Edge		Width: N3E-4 Delay: L1E-4 Transition Times: U1E-6V1E-6I	Scope: Leading edge and trailing edge time 1μs.
13			Leading Edge: U10E-6I	Scope: 10 μs leading edge.
14	CH1 Trailing Edge		Trailing Edge: V10E-6I	Scope: Trailing edge 10 μs.
15			Transition: U5E-9V5E-9I	Scope: 1 kHz pulse.
16	CH1 Frequency	Scope setting: Horizontal 10 ms/Div; vary as needed. Normal triggering.	Frequency: F100 Function: C2I	Scope: 100 Hz square.

Table 2-3. Initial Checkout (Continued)

Step	Test	Tester & Setup	Program	Desired Results
17	CH1 Period	Scope setting: Horizontal 10 ms/Div; vary as needed.	Period: S20E-3	Scope: Period 20 ms.
18	CH1 Double Pulse	Scope setting: Horizontal 0.2 ms/Div.	Frequency: F1E3 Width: N5E-5 Delay: L60E-6 Function: C1I	Scope: Double pulses, 60 μs apart.
19	CH1 Trigger Mode	Apply trigger pulse to TRIG IN. Trigger source: 0 to −1 V pulse, 1 kHz	Mode: B1 Frequency: F1E4 Trigger Format: K0 Function: C0I	Scope: A single pulse at the external trigger rate.
20	CH1 Gated Mode	Scope settings: Auto trigger. Horizontal 100 μs/Div	Trigger Format: K0 Function: C0 Width: N80E-6 Delay: L5E-8 Mode: B2I	Scope: A number of pulses occurring at the repetition rate during the active portion of the trigger signal.
21	CH1 Burst Mode	Trigger source: 0 to −1 V pulse, 10 Hz. Scope setting: Normal trigger Horizontal 2 ms/Div.	Frequency: F1E3 Function: C2 Mode: B3 Burst: R10I	Scope: A burst of ten 1 kHz pulse occurring at a 1 Hz rate.
22	Wake-Up State on CH2	Remove cable from 859 CH1 OUT and attach to 859 CH2 OUT. Scope settings: CH1 0.5 V/Div CH2 0.5 V/Div Horizontal 0.2 ms/Div External trigger	Output: ZG1C3G2P1C2I	Scope: 1 kHz, 1 Vp-p square wave
23	CH2 Output Levels	Scope setting: CH1, 5 V/Div	Upper Level: A5I	Scope: Level increases positively to 5 V
24			Lower Level: D-5I	Scope: Level increases negatively to −5V
25			Reprogram levels: A10D0I	Scope: 10V upper level, 0V lower level square wave
26	CH2 Normal/Complement Output		Width: N3E-4 Function: C0I	Scope: 1 kHz pulse.
27			Complement Output: O1I	Scope: Complement of previous pulse.
28			Output: O0I	Scope: Pulse width increases.
29	CH2 Width		Width: N1E-6I	Scope: Pulse width 1 μs.

Table 2-3. Initial Checkout (Continued)

Step	Test	Tester & Setup	Program	Desired Results
30			Width: N20E-6I	Scope: 20 μs wide pulse.
31	CH2 Delay		Delay: L1E-6I	Scope: Pulse delay 1 μs.
32	CH2 Leading Edge		Width: N3E-4 Delay: L1E-4 Transition Times: U1E-6V1E-6I.	Scope: Leading edge and trailing edge transition time 1 μs.
33			Leading Edge: U10E-6I	Scope: 10 μs leading edge.
34	CH2 Trailing Edge		Trailing Edge: V10E-6I	Scope: Trailing edge 10 μs.
35			Transition: U5E-9V5E-9I	Scope: 1 kHz pulse.
36	CH2 Frequency	Scope setting: Horizontal 10 ms/Div; vary as needed. Normal triggering.	Frequency: F100 Function: C2I	Scope: 100 Hz square.
37	CH2 Period	Scope setting: Horizontal 10 ms/Div; vary as needed.	Period: S20E-3	Scope: Period 20 ms.
38	CH2 Double Pulse	Scope setting: Horizontal 0.2 ms/Div.	Frequency: F1E3 Width: N5E-5 Delay: L60E-6 Function: C1I	Scope: Double pulses, 60 μs apart.
39	CH2 Trigger Mode	Apply trigger pulse to TRIG IN. Trigger source: 0 to −1 V pulse, 1 kHz	Mode: B1 Frequency: F1E4 Trigger Format: K0 Function: C0	Scope: A single pulse at the external trigger rate.
40	CH2 Gated Mode	Scope settings: Auto trigger. Horizontal 100 μs/Div	Trigger Format: K0 Function: C0 Width: N80E-6 Delay: L5E-8 Mode: B2I	Scope: A number of pulses occurring at the repetition rate during the active portion of the trigger signal.
41	CH2 Burst Mode	Trigger source: 0 to −1 V pulse, 10 Hz. Scope setting: Normal trigger Horizontal 2 ms/Div.	Frequency: F1E3 Function: C2 Mode: B3 Burst: R10I	Scope: A burst of ten 1 kHz pulse occurring at a 1 Hz rate.

Table 2-4. Acceptance Test Record (for Reproduction)

Location _____

QA Inspector _____

Date _____

Test From Table 2-3	Acceptable ✓ CH1 Step	CH2 Step
Self Test	1 _____	
Wake-Up State	2 _____	23 _____
Output Level		
Upper Level	3 _____	23 _____
Lower Level	4 _____	24 _____
Normal/Complement Output	6 _____	26 _____
Pulse Width	9 _____	29 _____
Pulse Delay	11 _____	31 _____
Transition Time		
Leading Edge	12 _____	32 _____
Trailing Edge	14 _____	34 _____
Frequency	16 _____	36 _____
Period	17 _____	37 _____
Double Pulse	18 _____	38 _____
Trigger Mode	19 _____	39 _____
Gated Mode	20 _____	40 _____
Burst Mode	21 _____	41 _____

Table 2-5. Performance Checkout

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
1	Rep Rate and Resolution at 5 Hz	Frequency Counter (figure 2-5) Read frequency at CH1 OUT, ±0.5 V Square Wave	Reset: Z CH1 ON: G1P1 Freq: F0.5I Read Freq, f1	480 mHz	520 mHz
			Freq: F0.501I Read Freq, f2	481 mHz	521 mHz
			f2 – f1	0.8 mHz	1.2 mHz
2	Rep Rate and resolution at 50 kHz		Freq: F5E4I Read Freq, f1	48.0 kHz	52.0 kHz
			Freq: F5.01E4I Read Freq, f2	48.1 kHz	52.1 kHz
			f2 – f1	90 Hz	120 Hz
3	Rep Rate and Resolution at 10 MHz		Freq: F1E7I Read Freq, f1	9.60 MHz	10.4 MHz
			Freq: F1.01E7I Read Freq, f2	9.61 MHz	10.41 MHz
			f2 – f1	8 kHz	12 kHz
4	CH 1 Pulse Width Rang and Resolution at 20 ns	Time Interval Probes and Counter (figure 2-5) Read Pulse Width at CH1 OUT, ±0.5V Square Wave	Freq: F1E6 Function, Pulse: C0 Pulse Width: N20E-9I Read Pulse Width, n1	16 ns	24 ns
			Pulse Width: N40E-9I Read Pulse Width, n2	36 ns	44 ns
			n2 – n1	16 ns	24 ns
5	CH1 Pulse Width Rang and Resolution at 100 μs		Freq, 1 kHz: F1E3 Function, Pulse: C0 Pulse Width: N99.5E-6I Read Pulse Width, n1	97.5 μs	101.5 μs
			Pulse Width: N1E-4I Read Pulse Width, n2	98.0 μs	102.0 μs
			n2 – n1	490 ns	510 ns

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
6	CH1 Pulse Width Range and Resolution at 1 ms	Time Interval Probes and Counter (figure 2-5) Read Pulse Width at CH1 OUT, ±0.5V Square Wave	Freq, 300 Hz: F300 Function, Pulse: C0 Pulse Width: N998E-6I Read Pulse Width, n1	978 μs	1018 μs
			Pulse Width: N999E-6I Read Pulse Width, n2	979 μs	1019 μs
			n2 – n1	900 ns	1100 ns
7	CH1 Pulse Width Range and Resolution at 100 ms		Freq, 3 Hz: F3 Function, Pulse: C0 Pulse Width: N98E-3I Read Pulse Width, n1	96.0 ms	100 ms
			Pulse Width: N99E-3I Read Pulse Width, n2	97.0 ms	101 ms
			n2 – n1	900 μs	1100 μs
8	CH1 Delay Range and Resolution at 20 ns	Time Interval Probes and Counter (figure 2-5) Read Pulse Delay between SYNC OUT and CH1 OUT	Freq: F1E6 Pulse Width: N40E-9 Pulse Delay: L20E-9I Read Pulse Delay, ℓ1	16 ns	24 ns
			Pulse Delay: L40E-9I Read Pulse Delay, ℓ2	36 ns	44 ns
			ℓ2 – ℓ1	16 ns	24 ns
9	CH1 Delay Range and Resolution at 1 ms		Freq: F300 Pulse Width: N50E-6 Pulse Delay: L998E-6I Read Pulse Delay, ℓ1	978 μs	1018 μs
			Pulse Delay: L999E-6I Read Pulse Delay, ℓ2	979 μs	1019 μs
			ℓ2 – ℓ1	900 ns	1100 ns
10	CH1 Delay Range and Resolution at 99 ms		Freq: F3 Pulse Width: N5E-3 Pulse Delay: L99E-3I Read Pulse Delay, ℓ1	97.0 ms	101 ms

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
10 (Cont)			Pulse Delay: L991E-4I Read Pulse Delay, ℓ2	97.1 ms	102 ms
			ℓ2 – ℓ1	90 μs	110 μs
11	CH1 Delay Range and Resolution at 1.599 s		Freq: F0.5 Pulse Width: N0.1 Pulse Delay: L1.598I Read Pulse Delay, ℓ1	1.566 s	1.631 s
			Pulse Delay: L1.599I Read Pulse Delay, ℓ2	1.567 s	1.632 s
			ℓ2 – ℓ1	900 μs	1100 μs
12	CH1 Rise Time Range and Resolution at 5 ns	Scope with Sampling Plug-in, or Time Interval Probes and Counter (figure 2-5)	Reset: ZG1P1C2 Level, ±5 V: A5D-5 Freq: F6E6 Leading Edge: U4E-9I Read Rise Time, u1	2 ns	6 ns
			Leading Edge: U9E-9I Read Rise Time, u2	7 ns	11 ns
			u2 – u1	3.5 ns	6.5 ns
13	CH1 Rise Time Range and Resolution at 190 ns		Freq: F1E6 Leading Edge: U190E-9I Read Rise Time, u1	175 ns	205 ns
			Leading Edge: U200E-9I Read Rise Time, u2	184 ns	216 ns
			u2 – u1	8.5 ns	11.5 ns
14	CH1 Rise Time Range and Resolution at 480 ns		Freq: F1E6 Leading Edge: U480E-9I Read Rise Time, u1	445 ns	515 ns
			Leading Edge: U500E-9I Read Rise Time, u2	463 ns	537 ns
			u2 – u1	17 ns	23 ns
15	CH1 Fall Time Range and Resolution at 5 ns		Reset: ZG1P1C2 Level, ±5 V: A5D-5 Freq: F6E6 Trailing Edge: V4E-9I Read Fall Time, v1	2 ns	6 ns

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
15 (Cont)			Trailing Edge: V9E-9I Read Fall Time, v2	7 ns	11 ns
			v2 – v1	3.5 ns	6.5 ns
16	CH1 Fall Time Range and Resolution at 190 ns		Freq: F1E6 Trailing Edge: V190E-9I Read Fall Time, v1	175 ns	205 ns
			Leading Edge: V200E-9I Read Fall Time, v2	184 ns	216 ns
			v2 – v1	8.5 ns	11.5 ns
17	CH1 Fall Time Range and Resolution at 480 ns		Freq: F1E6 Leading Edge: V480E-9I Read Fall Time, v1	445 ns	515 ns
			Leading Edge: V500E-9I Read Fall Time, v2	463 ns	537 ns
			v2 – v1	17 ns	23 ns
18	CH1 Over/Undershoot at 10 Vp-p	Scope with Sampling Plug-in (figure 2-4)	Reset: ZG1P1C2 Levels: A5D-5I Read Overshoot for positive peak	0 mV	<510 mV
			Read Overshoot for negative peak	0 mV	<510 mV
19	CH1 Over/Undershoot 2 Vp-p		Levels: A1D1I Read Overshoot for positive peak	0 mV	<110 mV
			Read Overshoot for negative peak	0 mV	<110 mV
20	CH1 Voltage Range and Accuracy at ±0.5 V	DVM (DC Mode) (figure 2-6)	Mode, Ext Width: B4 Output, Complement: O1 Trigger Format, Leading Edge: K0 Freq, 0.5 Hz: F5E-1 Levels: A.5D-.5I	+375 mV	+625 mV
			Output: O0I Read negative peak voltage	−625 mV	−375 mV
21	CH1 Voltage Range and Accuracy at ±5 V		Levels: A5D-5O1I Read positive peak voltage	+4.65 V	+5.35 V
			Output: O0I Read negative peak voltage	−5.35 V	−4.65 V
22	CH1 Voltage Range and Accuracy at 0 to +15 V		Levels: A15D0O1I Read positive peak voltage	+14.3 V	+15.7 V
			Output: O0I Read zero peak voltage	−150 mV	+150 mV

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
23	CH1 Voltage Range and Accuracy at 0 to −15 V	DVM (DC Mode) (figure 2-6)	Levels: A0D-15O0I Read negative peak voltage	−15.7 V	−14.3 V
			Output: O1I Read zero peak voltage	−150 mV	+150 mV
24	CH1 Voltage Range and Accuracy at 15 V 1 MΩ	Remove the 50Ω load and replace with a 1 MΩload	Levels: A7.5D0O1I Read positive peak voltage	+14.3 V	+15.7 V
			Output: O0I Read zero peak voltage	−150 mV	+150 mV
25	CH2 Pulse Width Range and Resolution at 20 ns	Time Interval Probes and Counter (figure 2-5) Read Pulse Width at CH2 OUT, ±0.5 V Square Wave	Disable CH1: G1C3I Freq: F1E6 Function, Pulse: C0 Pulse Width: N20E-9I Read Pulse Width, n1	16 ns	24 ns
			Pulse Width: N40E-9I Read Pulse Width, n2	36 ns	44 ns
			n2 − n1	16 ns	24 ns
26	CH2 Pulse Width and Resolution at 100 μs		Freq, 1 kHz: F1E3 Function, Pulse: C0 Pulse Width: N99.5E-6I Read Pulse Width, n1	97.5 μs	101.5 μs
			Pulse Width: N1E-4I Read Pulse Width, n2	98.0 μs	102.0 μs
			n2 − n1	490 ns	510 ns
27	CH2 Pulse Width Range and Resolution at 1 ms		Freq, 300 Hz: F300 Function, Pulse: C0 Pulse Width: N998E-6I Read Pulse Width, n1	978 μs	1018 μs
			Pulse Width: N999E-6I Read Pulse Width, n2	979 μs	1019 μs
			n2 − n1	900 ns	1100 ns
28	CH2 Pulse Width Range and Resolution at 100 ms		Freq, 3 Hz: F3 Function, Pulse: C0 Pulse Width: N98E-3I Read Pulse Width, n1	96.0 ms	100 ms
			Pulse Width: N99E-3I Read Pulse Width, n2	97.0 ms	101 ms

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
28 (Cont)			n2 – n1	900 μs	1100 μs
29	CH2 Delay Range and Resolution at 20 ns	Time Interval Probes and Counter (figure 2-5) Read Pulse Delay between SYNC OUT and CH2 OUT	Freq: F1E6 Pulse Width: N40E-9 Pulse Delay: L20E-9I Read Pulse Delay, ℓ1	16 ns	24 ns
			Pulse Delay: L40E-9I Read Pulse Delay, ℓ2	36 ns	44 ns
			ℓ2 – ℓ1	16 ns	24 ns
30	CH2 Delay Range and Resolution at 1 ms		Freq: F300 Pulse Width: N50E-6 Pulse Delay: L998E-6I Read Pulse Delay, ℓ1	978 μs	1018 μs
			Pulse Delay: L999E-6I Read Pulse Delay, ℓ2	979 μs	1019 μs
			ℓ2 – ℓ1	900 ns	1100 ns
31	CH2 Delay Range and Resolution at 99 ms		Freq: F3 Pulse Width: N5E-3 Pulse Delay: L99E-3I Read Pulse Delay, ℓ1	97.0 ms	101 ms
			Pulse Delay: L991E-4I Pluse Delay, ℓ2	97.1 ms	102 ms
			ℓ2 – ℓ1	90μs	110μs
32	CH2 Delay Range and Resolution at 1.599 s		Freq: F0.5 Pulse Width: N0.1 Pulse Delay: L1.598I Read Pulse Delay, ℓ1	1.566 s	1.631 s
			Pulse Delay: L1.599I Read Pulse Delay, ℓ2	1.567 s	1.632 s
			ℓ2 – ℓ1	900 μs	1100 μs
33	CH2 Rise Time Range Resolution at 5 ns	Scope with Sampling Plug-in, or Time Interval Probes and Counter (figure 2-5)	Reset: ZG2P1C2 Level, ± 5 V: A5D-5 Freq: F6E6 Leading Edge: U4E-9I Read Rise Time, u1	2 ns	6 ns
			Leading Edge: U9E-9I Read Rise Time, u2	7 ns	11 ns

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
33 (Cont)		Scope with Sampling Plug-in, or Time Interval Probes and Counter (figure 2-5)	u2 – u1	3.5 ns	6.5 ns
34	CH2 Rise Time Range and Resolution at 190 ns		Freq: F1E6 Leading Edge: U190E-9I Read Rise Time, u1	175 ns	205 ns
			Leading Edge: U200E-9I Read Rise Time, u2	184 ns	216 ns
			u2 – u1	8.5 ns	11.5 ns
35	CH2 Rise Time Range and Resolution at 480 ns		Freq: F1E6 Leading Edge: U480E-9I Read Rise Time, u1	445 ns	515 ns
			Leading Edge: U500E-9I Read Rise Time, u2	463 ns	537 ns
			u2 – u1	17 ns	23 ns
36	CH2 Fall Time Range and Resolution at 5 ns		Reset: ZG2P1C2 Level, ±5 V: A5D-5 Freq: F6E6 Trailing Edge: V4E-9I Read Fall Time, v1	2 ns	6 ns
37	CH2Fall Time Range amd Resolution at 190 ns		Freq: F1E6 Trailing Edge: V190E-9I Read Fall Time, v1	175 ns	205 ns
			Leading Edge: V200E-9I Read Fall Time, v2	184 ns	216 ns
			v2 – v1	8.5 ns	11.5 ns
38	CH2 Fall Time Range and Resolution at 480 ns		Freq: F1E6 Leading Edge: V480E-9I Read Fall Time, v1	445 ns	515 ns
			Leading Edge: V500E-9I Read Fall Time, v2	463 ns	537 ns
			v2 – v1	17 ns	23 ns
39	CH2 Over/Undershoot 10 Vp-p	Scope with Sampling Plug-in (figure 2-4)	Reset: ZG2P1C2 Levels: A5D-5I Read Overshoot for positive peak	0 mV	<510 mV
			Read Overshoot for negative peak	0 mV	<510 mV

Table 2-5. Performance Checkout (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
40	Ch2 Over/Undershoot at 2 Vp-p		Levels: A1D1I Read Overshoot for positive peak	0 mV	<110 mV
			Read Overshoot for negative peak	0 mV	<110 mV
41	CH2 Voltage Range and Accuracy at ±0.5V	DVM (DC Mode) (figure 2-6)	Mode, Ext Width: B4 Output, Complement: O1 Trigger Format, Leading Edge: K0 Freq, 0.5 Hz: F5E-1 Levels: A.5D-.5I Read positive peak voltage	+375 mV	+625 mV
			Output: O0I Read negative peak voltage	−625 mV	−375 mV
42	CH2 Voltage Range and Accuracy at ±5 V		Levels: A5D-5O1I Read positive peak voltage	+4.65 V	+5.35 V
			Output: O0I Read negative peak voltage	−5.35 V	−4.65 V
43	CH2 Voltage Range and Accuracy at 0 to +15 V		Levels: A15D0O1I Read positive peak voltage	+14.3 V	+15.7 V
			Output: O0I Read zero peak voltage	−150 mV	+150 mV
44	CH2 Voltage Range and Accuracy at 0 to −15 V		Levels: A0D-15O0I Read negative peak voltage	−15.7 V	−14.3 V
			Output: O1I Read zero peak voltage	−150 mV	+150 mV
45	CH2 Voltage Range and Accuracy at 15 V into 1 MΩ	Remove the 50Ω load and replace with a 1 MΩ load	Levels: A7.5D0O1I Read positive peak voltage	+14.3 V	+15.7 V
			Output: O0I Read zero peak voltage	−150 mV	+150 mV

Table 2-6. Performance Test Record

Test	Setting	Range Min	Range Max		Actual CH1 Step	Actual CH2 Step
Rep Rate and Resolution						
At 5 Hz	500 mHz	480 mHz	520 mHz	(f1)	**1** _____	_____
	501 mHz	481 mHz	521 mHz	(f2)	_____	_____
		0.8 mHz	1.2 mHz	(f2 – f1)	_____	_____
At 50 kHz	50 kHz	48.0 kHz	52.0 kHz	(f1)	**2** _____	_____
	50.1 kHz	48.1 kHz	52.1 kHz	(f2)	_____	_____
		90 Hz	120 Hz	(f2 – f1)	_____	_____
At 10 MHz	10 MHz	9.6 MHz	10.4 MHz	(f1)	**3** _____	_____
	10.1 MHz	9.61 MHz	10.41 MHz	(f2)	_____	_____
		8 kHz	12 kHz		_____	_____
Pulse Width Range and Resolution						
At 20 ns	20 ns	16 ns	24 ns	(n1)	**4** _____	**25** _____
	40 ns	36 ns	44 ns	(n2)	_____	_____
	16 ns	24 ns		(n2 – n1)	_____	_____
At 100 μs	99.5 μs	97.5 μs	101.5 μs	(n1)	**5** _____	**26** _____
	100 μs	98.0 μs	102.0 μs	(n2)	_____	_____
		490 ns	510 ns	(n2 – n1)	_____	_____
At 1 ms	998 μs	978 μs	1018 μs	(n1)	**6** _____	**27** _____
	999 μs	979 μs	1019 μs	(n2)	_____	_____
		900 ns	1100 ns	(n2 – n1)	_____	_____
At 100 ms	98 ms	96.0 ms	100 ms	(n1)	**7** _____	**28** _____
	99 ms	97.0 ms	101 ms	(n2)	_____	_____
		900 μs	1100 μs	(n2 – n1)	_____	_____
Pulse Delay Range and Resolution						
At 20 ns	20 ns	16 ns	24 ns	(ℓ1)	**8** _____	**29** _____
	40 ns	36 ns	44 ns	(ℓ2)	_____	_____
		16 ns	24 ns	(ℓ2 – ℓ1)	_____	_____
At 1 ms	998 μs	978 μs	1018 μs	(ℓ1)	**9** _____	**30** _____
	999 μs	979 μs	1019 μs	(ℓ2)	_____	_____
		900 ns	1100 ns	(ℓ2 – ℓ1)	_____	_____
At 99 ms	99 ms	97 ms	101 ms	(ℓ1)	**10** _____	**31** _____
	99.1 ms	97.1 ms	102 ms	(ℓ2)	_____	_____
		90 μs	110 μs	(ℓ2 – ℓ1)	_____	_____
At 1.599s	1.598s	1.566s	1.631s	(ℓ1)	**11** _____	**32** _____
	1.599s	1.567s	1.632s	(ℓ2)	_____	_____
		900 μs	1100 μs	(ℓ2 – ℓ1)	_____	_____
Pulse Rise Time Range and Resolution						
At 5 ns	4 ns	2 ns	6 ns	(u1)	**12** _____	**33** _____
	9 ns	7 ns	11 ns	(u2)		
		3.5 ns	6.5 ns	(u2 – u1)		

Table 2-6. Performance Test Record (Continued)

Test	Setting	Range Min	Range Max		Actual CH1 Step	Actual CH2 Step
Pulse Rise Time Range and Resolution (Cont)						
At 190 ns	190 ns	175 ns	205 ns	(u1)	**13** _____	**34** _____
	200 ns	184 ns	216 ns	(u2)	_____	_____
		8.5 ns	11.5 ns	(u2 – u1)	_____	_____
At 480 ns	480 ns	445 ns	515 ns	(u1)	**14** _____	**35** _____
	500 ns	463 ns	537 ns	(u2)	_____	_____
		17 ns	23 ns	(u2 – u1)	_____	_____
Rise Fall Time Range and Resolution						
At 5 ns	4 ns	2 ns	6 ns	(v1)	**15** _____	**36** _____
	9 ns	7 ns	11 ns	(v2)	_____	_____
		3.5 ns	6.5 ns	(v2 – v1)	_____	_____
At 190 ns	190 ns	175 ns	205 ns	(v1)	**16** _____	**37** _____
	200 ns	184 ns	216 ns	(v2)	_____	_____
		8.5 ns	11.5 ns	(v2 – v1)	_____	_____
At 480 ns	480 ns	445 ns	515 ns	(v1)	**17** _____	**38** _____
	500 ns	463 ns	537 ns	(v2)	_____	_____
		17 ns	23 ns	(v2 – v1)	_____	_____
Over/Undershoot						
At 10 Vp-p	10 Vp-p	0 mV	<510 mV	(+Pk)	**18** _____	**39** _____
		0 mV	<510 mV	(–Pk)	_____	_____
At 2 Vp-p	2 Vp-p	0 mV	<110 mV	(+Pk)	**19** _____	**40** _____
		0 mV	<110 mV	(–Pk)	_____	_____
Voltage Range and Accuracy						
At +0.5 V	1 Vp-p	+375 mV	+625 mV	(+Pk)	**20** _____	**41** _____
At –0.5 V	1 Vp-p	–625 mV	–375 mV	(–Pk)	_____	_____
At +5 V	10 Vp-p	+4.65 V	+5.35 V	(+Pk)	**21** _____	**42** _____
At –5 V	10 Vp-p	–5.35 V	–4.65 V	(–Pk)	_____	_____
At +15 V	+15, 0 V	+14.3 V	+15.7 V	(+Pk)	**22** _____	**43** _____
At 0 V	+15, 0 V	–150 mV	+150 mV	(–Pk)	_____	_____
At –15 V	–15, 0 V	–15.7 V	–14.3 V	(–Pk)	**23** _____	**44** _____
At 0 V	–15, 0 V	–150 mV	+150 mV	(+Pk)	_____	_____
At +15 V, 1MΩ	+7.5, 0 V	+14.3 V	+15.7 V	(+Pk)	**24** _____	**45** _____
At 0 V, 1MΩ	+7.5, 0 V	–150 mV	+150 mV	(–Pk)	_____	_____

3.8.3 Delay

L followed by its value in seconds denotes the pulse delay. Programmed pulse delays are from 0 to 1599 ms. Delay is relative to the rising edge of the sync output. For the single pulse, delay is measured to the 0% point of the pulse. Delays for the double pulse are measured to the 0% point of the second pulse.

Delay limitations are expressed in terms of the delay one shot pulse (see figure 3-4). When using delay, the delay pulse is an internal pulse triggered at the start of the pulse period or triggered by the acceptance of an external trigger. The completion of this delay pulse starts the output pulse, or, in the case of the double pulse, starts the second pulse. The delay pulse duty cycle cannot exceed 90% of the pulse period. Additionally, for delays less than 25 ns, the off time of the delay pulse cannot be less than 10 ns and for delays greater or equal to 25 ns, the off time cannot be less than 20 ns.

3.9.6 Sync Output

Sync output is provided at a BNC on the rear panel. The sync signal is 0V to approximately −1V into a 50Ω load. Sync output is a square wave in continuous mode. In other modes, sync width is determined by the time between the initial transition of the trigger signal through the preset trigger level to the trailing transition. For reference, refer to table 3-8, Output Signals Versus Modes, and table 3-9, System Delay Times. For best performance the sync output should be terminated into 50Ω.

3.9.7 Clock Output

Clock output is provided at a BNC on the rear panel. The clock signal is 0V to approximately −1V into a 50Ω load. Clock output is a square wave at the programmed repetition rate for continuous, gated and burst modes. In time interval modes, the clock rate is determined by the microprocessor. For reference, refer to table 3-8, Output Signals Versus Modes, and table 3-9, System Delay Times. For best performance the clock output should be terminated into 50Ω.

3.11.4 Talker

%T followed by its code sets the particular type of status message sent by the 859 when asked to talk on the GPIB. The codes may be **0** through **6** as follows.

0 Trigger Status. its format is:

H 1 EOS or **H 0** EOS

H — designates triggered status follows.
1 — Sent if the 859 is outputting a waveform in any mode except continuous.
0 — Sent if the **H 1** conditions are not true.
EOS — Terminator.

(The remaining section 3.11.4 is unchanged.)

3.11.7 GET Mode

%G followed by its code selects what actions occur when a Group Execute Trigger (GET) command is sent to the 859. The code must be **0**.

0 Upon receipt of GET, the programmed waveform values are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is not continuous. This is the same sequence of events that would occur if an execute, then a trigger action (**IJ**) were programmed, except that no error checking is done.

SECTION 4
CIRCUIT DESCRIPTION

4.3 DELAY AND WIDTH ONE SHOTS

Within the "3 digit ÷ N counter" in the DELAY ONE SHOT, Figure 4-8, the MSD is a 4 bit binary counter and the remaining 2 digits are BCD counters. The result is that the counter can count up to 1599 maximum, allowing the maximum delay to be 1.599 seconds.

(The remainder of section 4.3 is unchanged.)

4.6 TRIGGER COMPARATOR

The trigger comparator receives, processes and distributes the trigger signal to the appropriate circuit blocks. The intraconnection of the trigger comparator circuit block is shown in figure 4-14.

The input signal is processed by a high speed schmitt trigger to derive a fast rise time signal from random slope input signals. The dc trigger level is summed with the input signal. The input trigger level is set to − 400 mV, with 50Ω input impedance, to emulate the 10514 ECL receiver.

The trigger format logic, externally programmed by GPIB, selects the phase or slope on which the 859 will trigger.

The control logic circuit selects the external trigger, manual trigger or no trigger at all, depending upon the programmed mode of operation.

4.13 CLOCK OUTPUT

The clock output (see figure 4-3) is available as a separate output after being delayed in a Programmable Delay Line (PDL) and buffered by a 50Ω clock amplifier. The PDL is programmed by the CMOS bus to insert delays to the clock output in order to synchronize it with the 50Ω output amplifier as various modes and functions are selected. When loaded to ground with an external 50Ω terminator, this output provides a 0V to − 800 mV signal which emulates the 10192 ECL driver.

4.14 SYNC OUTPUT

Sync output (see figure 4-3) provides a time reference establishing the beginning of the delay. The output is available as a separate output after being delayed by a PDL and buffered by a 50Ω sync amplifier. The PDL is programmed by the CMOS bus to insert delays to the sync output amplifier in order to synchronize it with the 50Ω channel output amplifier as various modes and function are selected. When loaded to ground with an external 50Ω terminator, this output provides a 0V to − 800 mV signal which emulates the 10192 ELC driver.

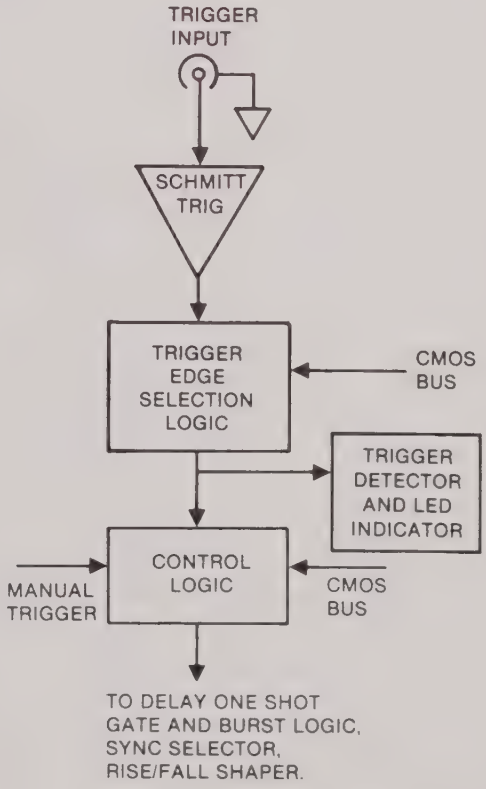


Figure 4-14. Trigger Comparator

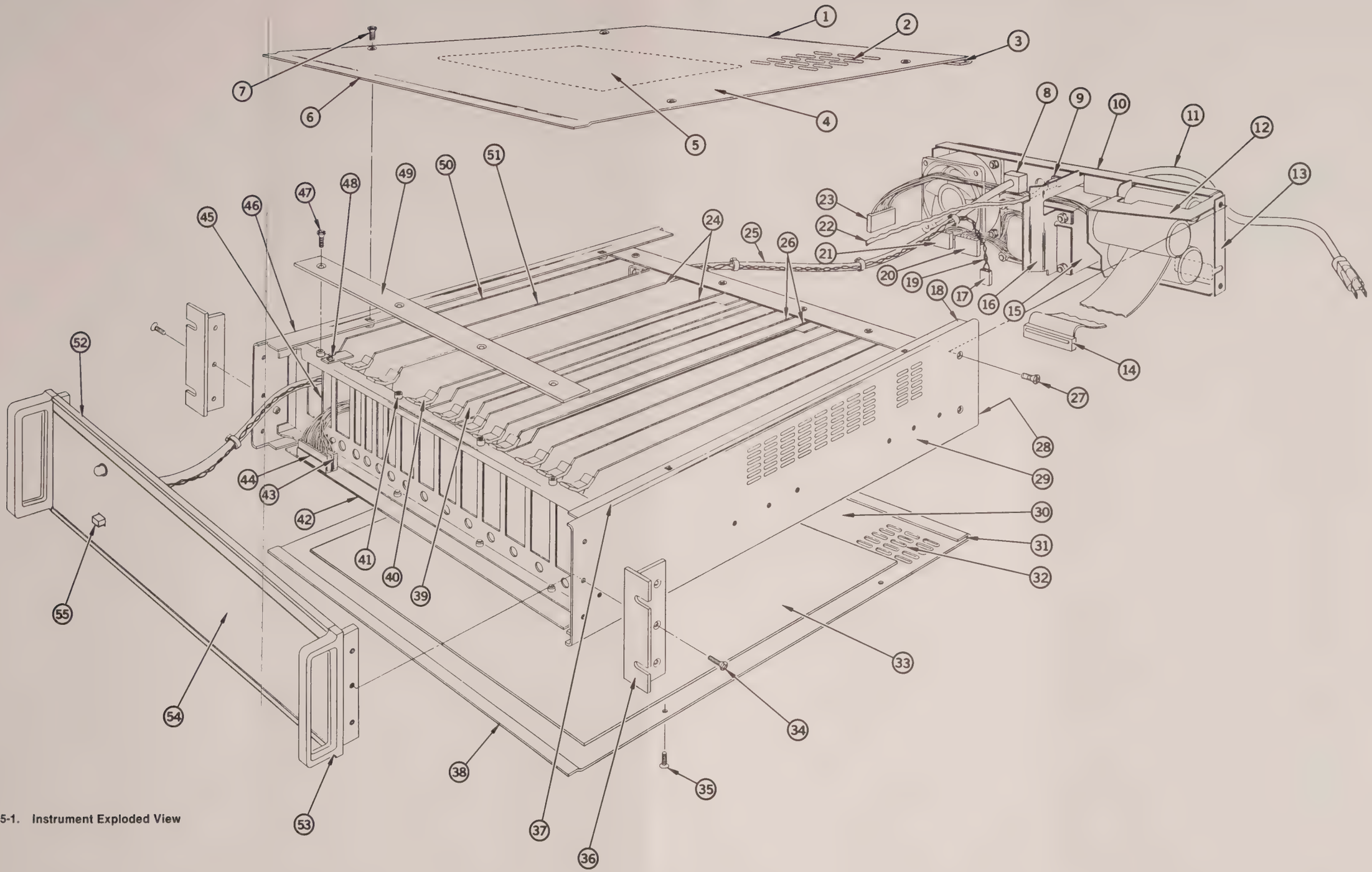


Figure 5-1. Instrument Exploded View

SECTION 5
TROUBLESHOOTING

5.9 REMOVAL AND INSTALLATION PROCEDURES

5.9.1 Top Cover

NOTE

Refer to figure 5-1 for this procedure.

WARNING

PRELIMINARY PROCEDURE: Remove power from unit with the Power On Off switch, (55), then disconnect power cable (11) at rear of instrument.

REMOVE

1. Remove 4 screws (7) holding top cover (4) to chassis (29).
2. Grasp rear of top cover (1) near BNC connectors (10) and pull back about 1/2 inch.
3. Remove top cover (4) by lifting straight up.

INSTALL

1. Place top cover (4) on chassis (29) with board location decal (5) facing plug-in boards, and vent holes (2) above rear panel mounted power supply capacitors (12).
2. Slide top cover (4) forward with front lip (6) in front panel groove (52) and rear chassis lip (18) in cover (3).
3. Fasten top cover (4) to chassis (29) using 4 screws (7).

5.9.2 Bottom Cover

NOTE

Refer to figure 5-1 for this procedure.

WARNING

PRELIMINARY PROCEDURE: Remove power from unit with the Power On Off switch, (55), then disconnect power cable (11) at rear of instrument.

REMOVE

1. Place instrument upside down.
2. Remove 4 screws (35) holding bottom cover (30) to chassis (29).
3. Grasp rear of bottom cover near transformer end bell and pull back about 1/2 inch.
4. Remove bottom cover (30) by lifting straight up.

INSTALL

1. Place instrument upside down.
2. Place bottom cover (30) on chassis (29) with insulator (33) facing mother board (42) and vent holes (32) above power supply capacitors (12).
3. Slide bottom cover (30) forward with front lip (38) in front panel groove (53) and rear chassis lip (28) in cover (31).
4. Fasten bottom cover (30) to chassis (29) using 4 screws (35).

5.9.3 Retainer Bars

NOTE

Refer to figure 5-1 for this procedure.

REMOVE

1. Remove top cover (4) (paragraph 5.9.1).
2. Remove 4 screws (47) holding each retainer bar (49) to chassis (29).
3. Remove retainer bars (49) by lifting straight up.

INSTALL

1. Place retainer bars (49) above board ejectors (40) and line up with threaded standoffs (41).

NOTE

When properly installed, retainer bars (49) are centered between the chassis sides (37, 46), and cover board ejectors (40).

2. Fasten retainer bars (49) to chassis (29) using 4 screws (47).

3. Fasten top cover (4) to chassis (29) (paragraph 5.9.1).

5.9.4 Front Panel Assembly

NOTE

Refer to figure 5-1 for this procedure.

REMOVE

1. Remove top cover (4) from chassis (29) (paragraph 5.9.1).
2. Remove all six screws (34) holding front panel rack mounting brackets (36) to front of chassis (29).
3. Carefully slide front panel (54) away from chassis (29).

NOTE

Do the following steps only if the front panel (54) is to be completely removed.

4. Remove HI AMP power supply board (50) (see paragraph 5.9.6).
5. Remove power switch cable (25) and power light wires (19) from clips (figure 5-4 #14) mounted on inside of chassis (29).
6. Disconnect larger of two connectors (8) from rear panel (13).
7. Remove both Delay and Width boards (26) from chassis (29) (paragraph 5.9.7).
8. Disconnect J20 connector (17) from mother board (42).
9. Remove power switch cable (25) and power light wires (19) from chassis (29).
10. Lift front panel (54) away from chassis (29).

INSTALL

NOTE

If the front panel (54) was not completely removed, begin with step 11.

1. Place front panel (54) near front of chassis (29).
2. Feed power switch cable (25) and power light wires (19) through extreme left of chassis (29).
3. Remove four screws (27) holding rear panel (13) to chassis (29).
4. Slide rear panel (13) back about 1/4 inch and push power light wires (19) under transformer (15) and bracket (16).
5. Connect J20 connector (17) to mother board (42).
6. Being carefull not to pinch any wires, slide rear panel (13) into rear of chassis (29) and secure with 4 screws (27).
7. Install both Delay and Width boards (26) in chassis (29) (paragraph 5.9.7).
8. Connect larger of two connectors (8) to rear panel (13).
9. Slip power switch cable (25) and power light wires (19) into clips (figure 5-4 #14) mounted on inside of chassis (29).
10. Install HI AMP power supply board (50) (paragraph 5.9.6).
11. Carefully slide front panel (54) into front of chassis (29).
12. Secure front panel rack mounting brackets (36) with 6 screws (34).
13. Mount retainer bars (49) (paragraph 5.9.3).
14. Fasten top cover (4) (paragraph 5.9.1).

5.9.5 Rear Panel Assembly

NOTE

Refer to figure 5-1 for this procedure.

REMOVE

1. Remove bottom cover (30) (paragraph 5.9.2).

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all rear panel mounted capacitors (12) to ground to prevent electrical shock.

2. Remove top cover (4) (paragraph 5.9.1).
3. Remove burst counter board (39) (paragraph 5.9.7).
4. Remove both output amplifier boards (24) (paragraph 5.9.7).
5. Cut ty-wrap holding burst counter coax cables to chassis (29).
6. Disconnect both connectors (8, 9) at top of rear panel (13).
7. Remove all four screws (27) holding rear panel (13) to rear of chassis (29).
8. Carefully slide rear panel (13) clear of chassis (29).
9. Remove connector (23) from rear of HI AMP power supply board (50).

10. Disconnect ribbon connector (14) at rear of mother board (42).
11. Disconnect the two connectors (20, 21) from rear of mother board (42).
12. Pull all rear panel wires clear of chassis (29).
13. Lift rear panel (13) away from chassis (29).

INSTALL

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all rear panel mounted capacitors to ground to prevent electrical shock.

1. Place rear panel (13) near rear of chassis (29).
2. Connect ribbon connector (14) to rear of mother board (42).
3. Connect the two connectors (20, 21) to rear of mother board (42) (match numbers printed on connector with those on rear of board next to connector pins).
4. Connect connector (23) to rear of HI AMP power supply board (50).
5. Connect both connectors (8, 9) at top of rear panel (13).

CAUTION

In the following step, care must be taken not to pinch wires between rear panel (13) and chassis (29).

6. Carefully slide rear panel (13) into rear of chassis (29).
7. Secure rear panel (13) to chassis (29) with four screws (27).
8. Secure burst counter coax cables to chassis (29) with ty-wrap.
9. Install bottom cover (30) on chassis (29) (paragraph 5.9.2).
10. Install both output amplifier boards (24) in chassis (29) (paragraph 5.9.7).
11. Install burst counter board (39) in chassis (29) (paragraph 5.9.7).
12. Fasten retainer bars (49) to chassis (29) (paragraph 5.9.3).
13. Mount top cover (4) to chassis (29) (paragraph 5.9.1).

5.9.6 HI AMP Power Supply Board

NOTE

Refer to figure 5-1 for this procedure.

REMOVE

1. Remove top cover (4) (paragraph 5.9.1).
2. Remove rack mounting brackets (36) held by 6 screws (34).
3. Slide front panel (54) away from chassis (29).
4. Remove J16 (43) and J17 (44) from front of mother board (42).
5. Disconnect the smaller of two rear panel connectors (9).
6. Disconnect connector (23) from rear of HI AMP power supply board (50).
7. Remove LO AMP power supply board (51) from chassis (29) (paragraph 5.9.7).
8. Remove screws (48) from each end of HI AMP power supply board (50).
9. Remove HI AMP power supply board (50) from chassis (29).

INSTALL

1. Feed J16 (43) and J17 (44) connectors through front left opening in chassis (45).
2. Carefully slide HI AMP power supply board (50) into chassis (29) and both board brackets at bottom of chassis (29).
3. Secure HI AMP power supply board (50) to chassis (29) with two screws (48).
4. Feed thermostat cable (22) through rear chassis opening nearest HI AMP power supply board (50).
5. Connect the smaller of two rear panel connectors (9).
6. Connect connector P12 (23) to HI AMP power supply board (50).
7. Connect J16 (43) and J17 (44) to front of mother board (42).
8. Verify that thermostat cable (22) is against HI AMP power supply board (50).
9. Install LO AMP power supply board (51) into chassis (29) (paragraph 5.9.7).
10. Slide front panel (54) into chassis (29).
11. Secure front panel rack mounting brackets (36) with 6 screws (34).

12. Mount retainer bars (49) (paragraph 5.9.3).
13. Secure top cover (4) (paragraph 5.9.1).

5.9.7 Plug-in PC Boards

NOTE

Refer to figure 5-2 for this procedure.

REMOVE

CAUTION

PC boards contain parts which are sensitive to electrostatic voltages. Grounding precautions must be used when handling these boards to prevent damage to components.

1. Remove top cover (1) (paragraph 5.9.1).
2. Remove retainer bars (7) (paragraph 5.9.3).

NOTE

Output amplifier boards and delay/width boards are calibrated together for each channel, therefore if both are removed at the same time, label each board for correct installation.

3. Lift end of PC Board ejectors (6) pointing toward center of unit (note detail 'A').

NOTE

If used, disconnect coax connectors (8) from front of board (10) during next step.

4. Remove board (10) by lifting straight up.

INSTALL

CAUTION

PC boards contain parts which are sensitive to electrostatic voltages. Grounding precautions must be used when handling these boards to prevent damage to components.

CAUTION

To prevent edge connector solder joints from being fractured, do not attempt to install any plug-in board (10) unless the bottom cover is installed.

1. With instrument front panel (5) at left, position plug-in board (10) with component side toward operator and PC board ejectors (6) on top of board.

NOTE

If used, connect coax connectors (8) to front of board (10) (note coax markings) during next step.

2. Insert PC board edges (2) into plastic PC board guides (3) (note PC board guide (3), and ejector (6) color code), then lower board (10) into edge connector on mother board until properly seated.
3. Install retainer bars (7) (paragraph 5.9.3).
4. Fasten top cover (1) to chassis (4) (paragraph 5.9.1).

5.9.8 Delay & Width Piggy Boards

NOTE

Refer to figure 5-3 for this procedure.

REMOVE

1. Remove Delay & Width board (5) from chassis (paragraph 5.9.7).
2. Remove 5 screws and lockwashers across top, and 4 screws (3) and lockwashers (2) across bottom of Delay & Width board (5).
3. Without damaging the connector pins (4), carefully separate the Delay & Width board (5) from the Delay & Width Piggy board (6).

INSTALL

1. Without damaging the connector pins (4), carefully join the Delay & Width board (5) to the Delay & Width Piggy board (6).
2. Install 5 screws and lockwashers across top and 4 screws (3) and lockwashers (2) across bottom of Delay & Width board (5).
3. Install Delay & Width board (5) in chassis (paragraph 5.9.7).

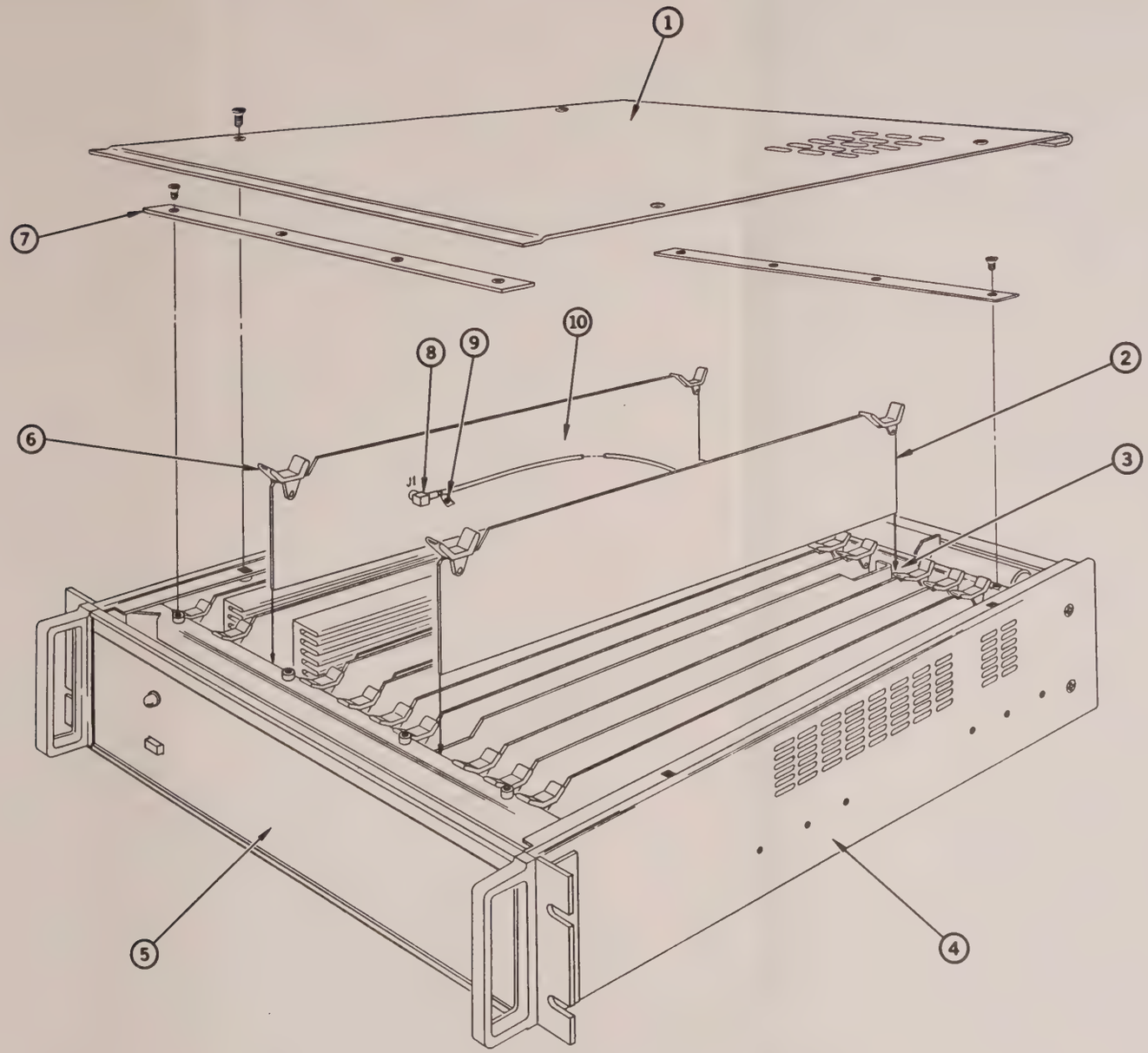
5.9.9 Mother Board

NOTE

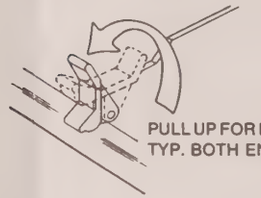
Refer to figure 5-4 for this procedure.

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all capacitors to ground to prevent electrical shock.



DETAIL "A"
TYP. PC BD. REMOVAL



PULL UP FOR PC BD. REMOVAL
TYP. BOTH ENDS.

Figure 5-2. PC Board Replacement

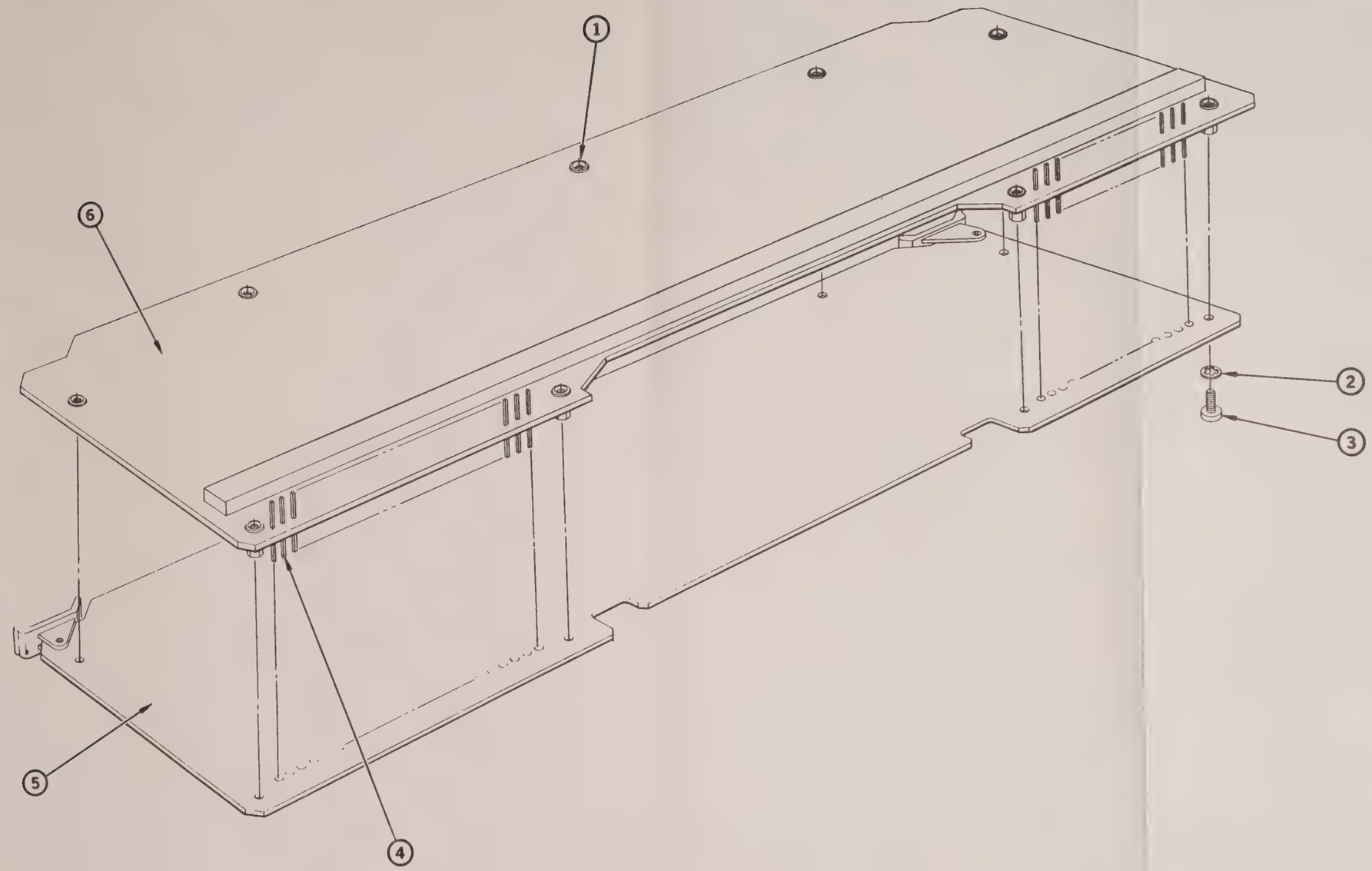


Figure 5-3. Delay & Width Piggy Board Replacement

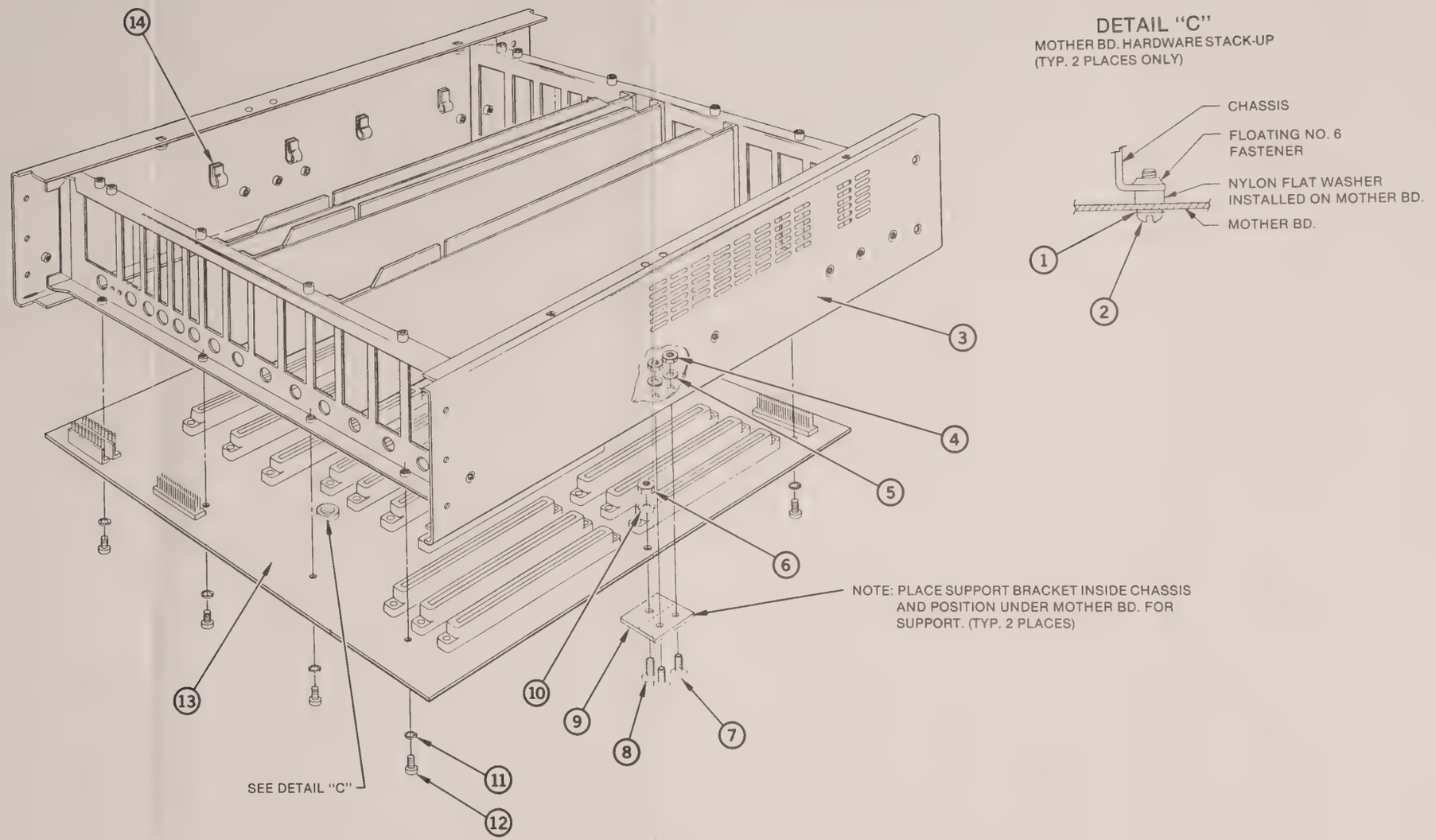


Figure 5-4. Mother Board Replacement

1. Remove top cover (paragraph 5.9.1).
2. Remove retainer bars (paragraph 5.9.3).
3. Remove all plug-in boards (paragraphs 5.9.6 and 5.9.7).
4. Disconnect P14 (figure 5-1 #21) and P15 (figure 5-1 #20) from rear of mother board (13).
5. Disconnect P16 (figure 5-1 #43) and P17 (figure 5-1 #44) from front of mother board (13).
6. Disconnect the indicator light connector (figure 5-1 #17) from rear of mother board (13).
7. Remove bottom cover (paragraph 5.9.2).
8. Carefully remove ribbon connector (figure 5-1 #14) from rear of mother board (13).
9. Remove 2 screws (7), lock washers (5) and nuts (4) securing mother board mounting tabs (9) to each side of mother board (13).
10. Remove one mother board mounting tab (9) held by screw (8), flat washer (10) and locknut (6).
11. Remove all 8 screws (12) and lockwashers (11) from front and rear of mother board (13).
12. Remove 2 screws (2) and flat washers (1) from near center of mother board (13).
13. Lift mother board (13) away from chassis (3).

INSTALL

1. With instrument upside down, lay mother board (13) on bottom of chassis (3).
2. Connect ribbon connector (figure 5-1 #14) to rear of mother board (13).
3. Connect indicator light connector (figure 5-1 #17) to rear of mother board (13).
4. Connect the two connectors (figure 5-1 #20, #21) to rear of mother board (13).
5. Verify rear panel wires are positioned properly.
6. Install but do not tighten 8 screws (12) and lockwashers (11) at front and rear of mother board (13).
7. Install but do not tighten 2 screws (2) and flat washers (1) near center of mother board (13).
8. Install but do not tighten mother board mounting tab (9) to chassis (3) using screw (8), flat washer (10) and locknut (6).
9. Mount and tighten both mother board mounting tabs (9) to chassis (3) with 2 screws (7), lock washers (5) and nuts (4).
10. Tighten 8 screws (12) at front and rear of mother board (13), 2 screws (2) near center of mother board (13) and screw (8) holding mother board (13) to mounting tab (9).
11. Fasten bottom cover (paragraph 5.9.2).
12. Install all plug-in boards (paragraphs 5.9.6 and 5.9.7).
13. Fasten retainer bars (paragraph 5.9.3).
14. Mount top cover (paragraph 5.9.1).

5.9.10 Clock Oscillator Shield.

NOTE

Refer to figure 5-5 for this procedure.

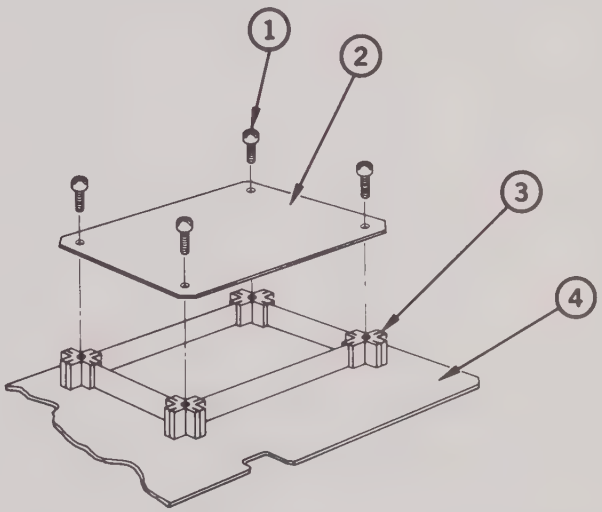


Figure 5-5. Clock Oscillator Shield Replacement

REMOVE

1. Remove clock oscillator board (4) from chassis (paragraph 5.9.7).
2. Remove 4 screws (1) securing shield (2) to standoffs (3).
3. Lift shield (2) away from clock oscillator board (4).

INSTALL

1. Secure shield (2) to standoffs (3) with 4 screws (1).
2. Install clock oscillator board (4) in chassis (paragraph 5.9.7).

5.9.11 PC Board Ejectors

NOTE

Refer to figure 5-6 for this procedure.

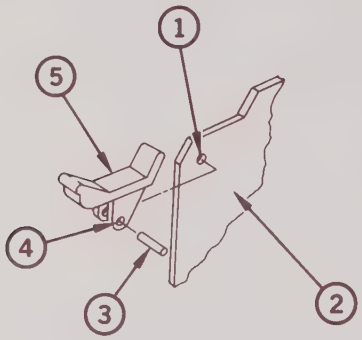


Figure 5-6. PC Board Ejector Replacement

REMOVE

1. Remove PC Board (2) from chassis (see paragraph 5.9.7).
2. Lay board (2) on a flat surface with space available for the roll pin (3) to be extracted.
3. Using a scribe and hammer, force out the roll pin (3).

INSTALL

1. Verify that ejector (5) points in correct direction and holes (1, 4) line up properly.
2. With a pair of slip-joint pliers, insert the roll pin (3) into one side of ejector (5), then squeeze both sides of the ejector (5) to force the roll pin (3) in place.
3. Install PC board (2) in chassis (paragraph 5.9.7).

5.9.12 Power Switch

NOTE

Refer to figure 5-7 for this procedure.

REMOVE

1. Remove top cover (paragraph 5.9.1).
2. Partially move front panel (1) from chassis (paragraph 5.9.4).
3. Disconnect larger of two connectors (figure 5-1 #8) on rear panel (figure 5-1 #13).
4. Remove HI AMP power supply board (paragraph 5.9.6).
5. Remove power switch cable (figure 5-1 #25) from clips (figure 5-4 #14) mounted on inside of chassis (figure 5-1 #29).
6. Remove power switch cable (figure 5-1 #25) from chassis (figure 5-1 #29).
7. Remove 2 screws (9) and washers (10) holding power switch mounting bracket (13) to front panel (1).
8. Remove 2 screws (11), lockwashers (8) and nuts (7) holding power switch (6) to power switch mounting bracket (13).
9. Remove power switch (6) from power switch mounting bracket (13).

INSTALL

1. Secure power switch (6) on power switch mounting bracket (13) with 2 screws (12), lockwashers (8) and nuts (7).
2. Secure power switch mounting bracket (13), power switch cable bracket (11) and ground wire lug (14) to front panel (1) with 2 screws (9) and washers (10).
3. Feed power switch cable (figure 5-1 #25) through extreme left of chassis (figure 5-1 #45) and slip into clips (figure 5-4 #14) mounted on inside wall of chassis.
4. Install HI AMP power supply board (paragraph 5.9.6).
5. Connect larger of two connectors (figure 5-1 #8) on rear panel (figure 5-1 #13).
6. Install front panel (1) into chassis (paragraph 5.9.4).
7. Fasten retainer bars (paragraph 5.9.3).
8. Secure top cover to chassis (paragraph 5.9.1).

5.9.13 Power On Indicator Light

NOTE

Refer to figure 5-7 for this procedure.

REMOVE

1. Unscrew indicator lens (5) from front panel (1).
2. Carefully remove the light bulb (4) from the indicator lens (5).

Install

1. Insert a light bulb (4) into the indicator lens (5).
2. Screw indicator lens (5) into front panel (1).

5.9.14 Front Panel Handles

NOTE

Refer to figure 5-7 for this procedure.

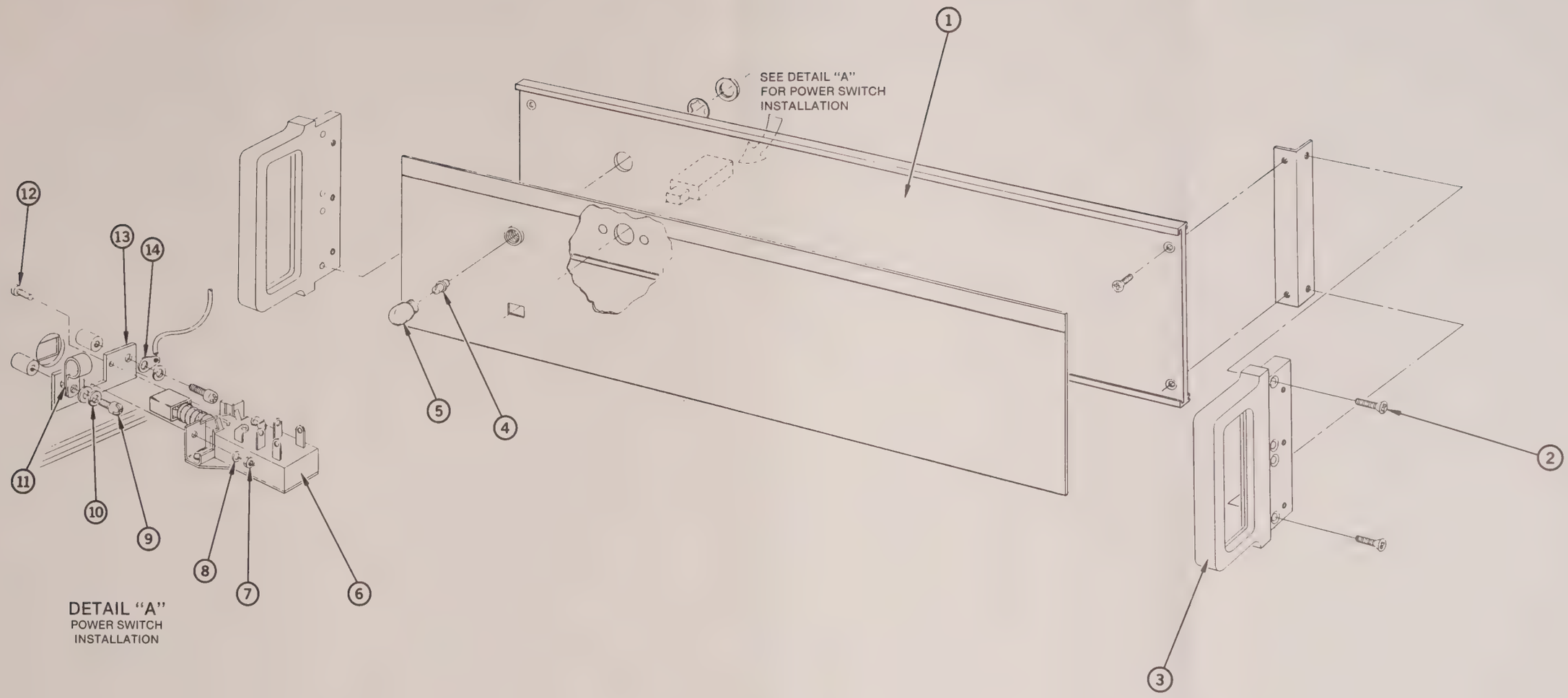


Figure 5-7. Front Panel Component Replacement

REMOVE

1. Remove top cover (paragraph 5.9.1).
2. Remove front panel assembly (1) from chassis (paragraph 5.9.4).
3. Remove 2 screws (2) holding each handle (3) to front panel (1).

INSTALL

1. Secure each handle (3) to front panel (1) with 2 screws (2).
2. Mount front panel assembly (1) to chassis (paragraph 5.9.4).
3. Install top cover (paragraph 5.9.1).

5.9.15 Electrolytic Capacitors C1, C2 and C5

NOTE

Refer to figure 5-8 for this procedure.

NOTE

This task is nearly identical for electrolytic capacitors C1 (5), C2 (9) and C5 (4). Only C1 (5) is shown.

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all rear panel mounted capacitors to ground to prevent electrical shock.

REMOVE

1. Remove rear panel (25) from chassis (paragraph 5.9.5).
2. Remove 3 screws (23) and lockwashers (24) from rear panel capacitor mounting bracket (8).
3. Remove 3 screws (19) and lockwashers (18) holding rear panel power diode bracket (14).
4. Remove 2 screws (11), solder lugs (13) and lock washers (12) from capacitor connections.
5. Loosen clamp (7) by turning screw (6) and remove capacitor.

INSTALL

WARNING

The electrolytic capacitor must be installed properly or component damage and a dangerous condition will result.

Connect as follows:

Capacitor C1 (5) negative lead connected to ground plate (10).

Capacitors C2 (9) and C5 (4) positive leads connected to ground plate (10).

1. Secure capacitor (5) inside clamp (7) by tightening screw (6).
2. Connect capacitor to circuit with 2 screws (11), solder lugs (13) and lock washers (12).
3. Mount power diode bracket (14) to rear panel (25) with 3 screws (19) and lockwashers (18).
4. Mount capacitor bracket (8) to rear panel (25) with 3 screws (23) and lockwashers (24).
5. Mount rear panel (25) to chassis (paragraph 5.9.5).
6. Install bottom cover (paragraph 5.9.2).
7. Install plug-in PC boards in chassis (paragraph 5.9.7).
8. Fasten retainer bars (paragraph 5.9.3).
9. Secure top cover to chassis (paragraph 5.9.1).

5.9.16 GPIB Ribbon Assembly

NOTE

Refer to figure 5-8 for this procedure.

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all rear panel mounted capacitors to ground to prevent electrical shock.

REMOVE

1. Remove rear panel (25) from chassis (paragraph 5.9.5).
2. Remove rear panel capacitor bracket (8) held by 3 screws (23) and lockwashers (24).
3. Remove rear panel GPIB connector (1) held by 2 screws (20), lockwashers (16) and nuts (15).
4. Remove 2 screws (21) and lockwashers (22) holding rear panel GPIB address selector (3).
5. Feed ribbon assembly (2) through GPIB connector opening (17) in rear panel (25).

INSTALL

1. Feed ribbon assembly (2) through GPIB connector opening (17) from exterior of rear panel (25).

2. Secure GPIB address selector (3) to rear panel (25) with 2 screws (21) and lockwashers (22).
3. Mount GPIB connector (1) to rear panel (25) with 2 screws (20), lockwashers (16) and nuts (15).
4. Feed ribbon (2) through C1 (5) and C2 (9), then secure capacitor bracket (8) to rear panel (25) with 3 screws (23) and lockwashers (24).
5. Mount rear panel (25) to chassis (paragraph 5.9.5).
6. Install bottom cover (paragraph 5.9.2).
7. Install plug-in PC boards in chassis (paragraph 5.9.7).
8. Fasten retainer bars (paragraph 5.9.3).
9. Secure top cover to chassis (paragraph 5.9.1).

5.9.17 BNC Connectors J23 and J24

NOTE

Refer to figure 5-9 for this procedure.

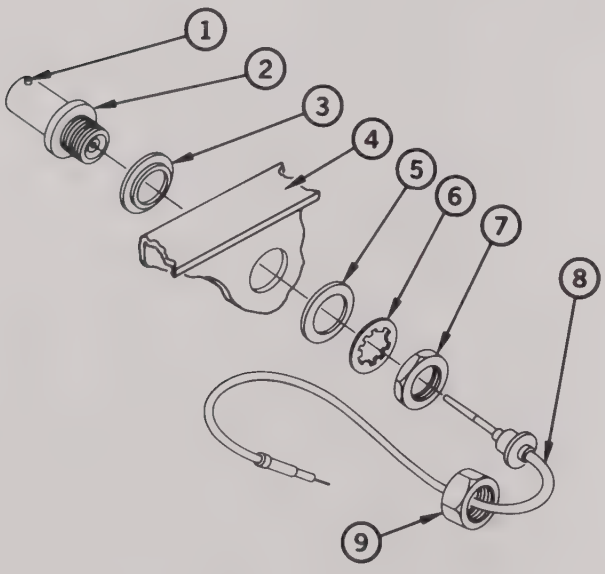


Figure 5-9 BNC Connector Replacement

NOTE

This task is the same for BNC connectors J23 and J24.

REMOVE

1. Remove top cover (see paragraph 5.9.1).

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all rear panel mounted capacitors to ground to prevent electrical shock.

2. Using a 1/2 inch open end wrench, loosen and slide the large nut (9) away from the connector (2).
3. Remove cable assembly (8) from connector (2).

NOTE

Replace cable assembly (8) if damaged.

4. Loosen and remove the smaller nut (7), lockwasher (6) and shoulder washer (5) holding connector (2).
5. Remove connector (2) and second shoulder washer (3) from rear panel (4).

INSTALL

1. Insert connector (2) through shoulder washer (3) into rear panel (4) with tabs (1) in the vertical position.
2. Install another shoulder washer (5), lockwasher (6) and smaller nut (7) on connector (2). Tighten using a 1/2 inch open end wrench.
3. Insert pin of cable assembly (8) into rear of connector (2).
4. Secure cable assembly (8) with large nut (9).
5. Install top cover (see paragraph 5.9.1).

5.9.18 Fan Filter

NOTE

Refer to figure 5-10 for this procedure.

WARNING

PRELIMINARY PROCEDURE: Remove power from unit with the Power On Off switch, (figure 5-1 #55), then disconnect power cable (figure 5-1 #11) at rear of instrument.

REMOVE

1. Remove screen cover (5) held by 2 screws (1) from rear panel (3).
2. Remove fan filter (4).

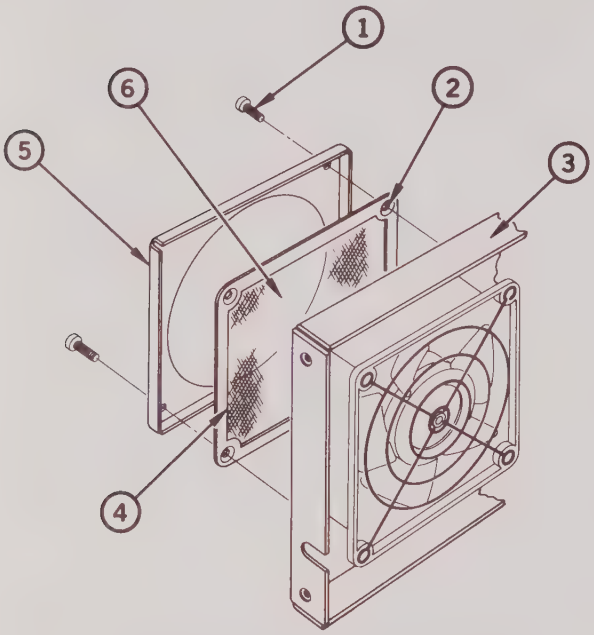


Figure 5-10. Fan Filter Replacement

INSTALL

1. Mount fan filter (4) in screen cover (5) with filter ribbing (6) vertical and corner projections (2) against screen cover (5).
2. Secure filter assembly (4, 5) to rear panel (3) with 2 screws (1).

5.9.19 Large HI AMP Power Supply Heat Sink

NOTE

Refer to figure 5-11 for this procedure.

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all capacitors to ground to prevent electrical shock.

REMOVE

1. Remove HI AMP power supply board (5) from chassis (paragraph 5.9.6).
2. Unsolder wires from E28 (22), E29 (24), E30 (2) and E31 (4).
3. Remove screw (21), lockwasher (20), flat washer (19) and shoulder washer (18) holding power transistor Q8 (17) to heat sink (7) (paragraph 5.9.22).
4. Remove power transistors Q2 (10) and Q6 held to heat sink (7) with screws (12) and lockwashers (11).
5. Remove all 6 screws (15) and lockwashers (16) holding heat sink (7) to HI AMP board (5).
6. Carefully lift heat sink (7) away from HI AMP board (5) while feeding thermostat cable (1) through hole (25) in PC board (5).

INSTALL

1. From foil side of PC board (5), feed thermostat cable (1) through hole (25).
2. Feed 4 wires (6) from 10 watt resistors R2 (8) and R16 (13) through openings (3, 23) to component side of PC board (5).
3. Carefully mount heat sink (7) on HI AMP board (5) and secure with 6 screws (15) and lockwashers (16).
4. Coat back of power transistors Q2 (2N5883) (10) and Q6 (2N5885) and insulators (9) with thermal compound (Wakefield #120-2), then mount to heat sink (7).
5. Secure power transistors Q2 (10) and Q6 to heat sink (7) with screws (12) and lockwashers (11).

CAUTION

In the following step, ensure that the shoulder washer (18) fits properly into the voltage regulator hole (14) to prevent shorting the regulator (17) to ground.

6. Secure power transistor Q8 (17) to heat sink (7) with screw (21), lockwasher (20), flat washer (19) and shoulder washer (18) (paragraph 5.9.22).
7. Solder left lead of R16 (13) to E28 (22), right lead of R16 (13) to E29 (24), left lead of R2 (8) to E30 (2) and right lead of R2 (8) to E31 (4) on HI AMP board (5).
8. Insert HI AMP power supply board (5) into chassis (paragraph 5.9.6).
9. Install LO AMP power supply board into chassis (paragraph 5.9.7).
10. Fasten retainer bars (paragraph 5.9.3).
11. Secure top cover to chassis (paragraph 5.9.1).

5.9.20 Output Amplifier Heat Sink

NOTE

Refer to figure 5-12 for this procedure.

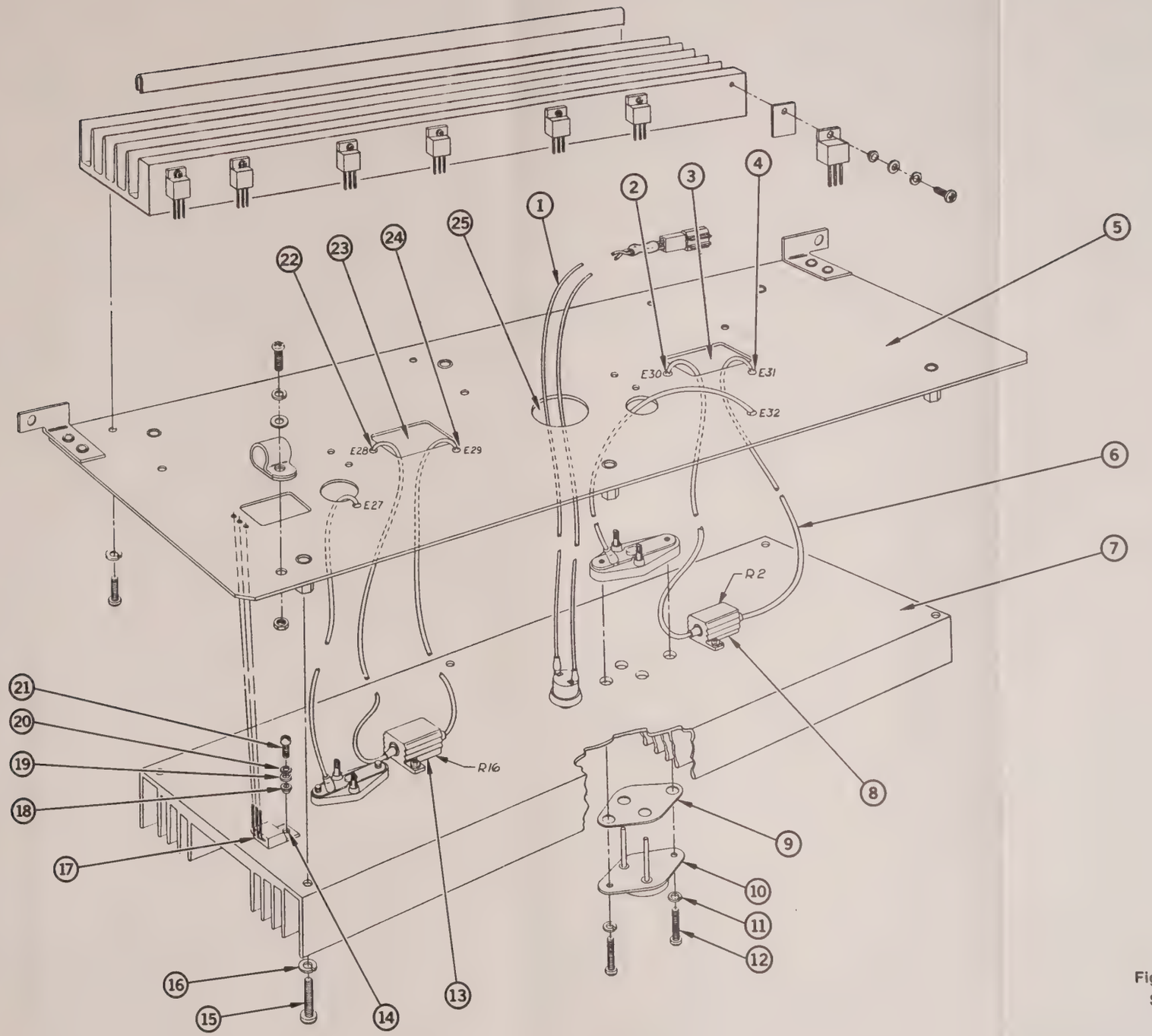


Figure 5-11. Large HI AMP Power Supply Heat Sink Replacement

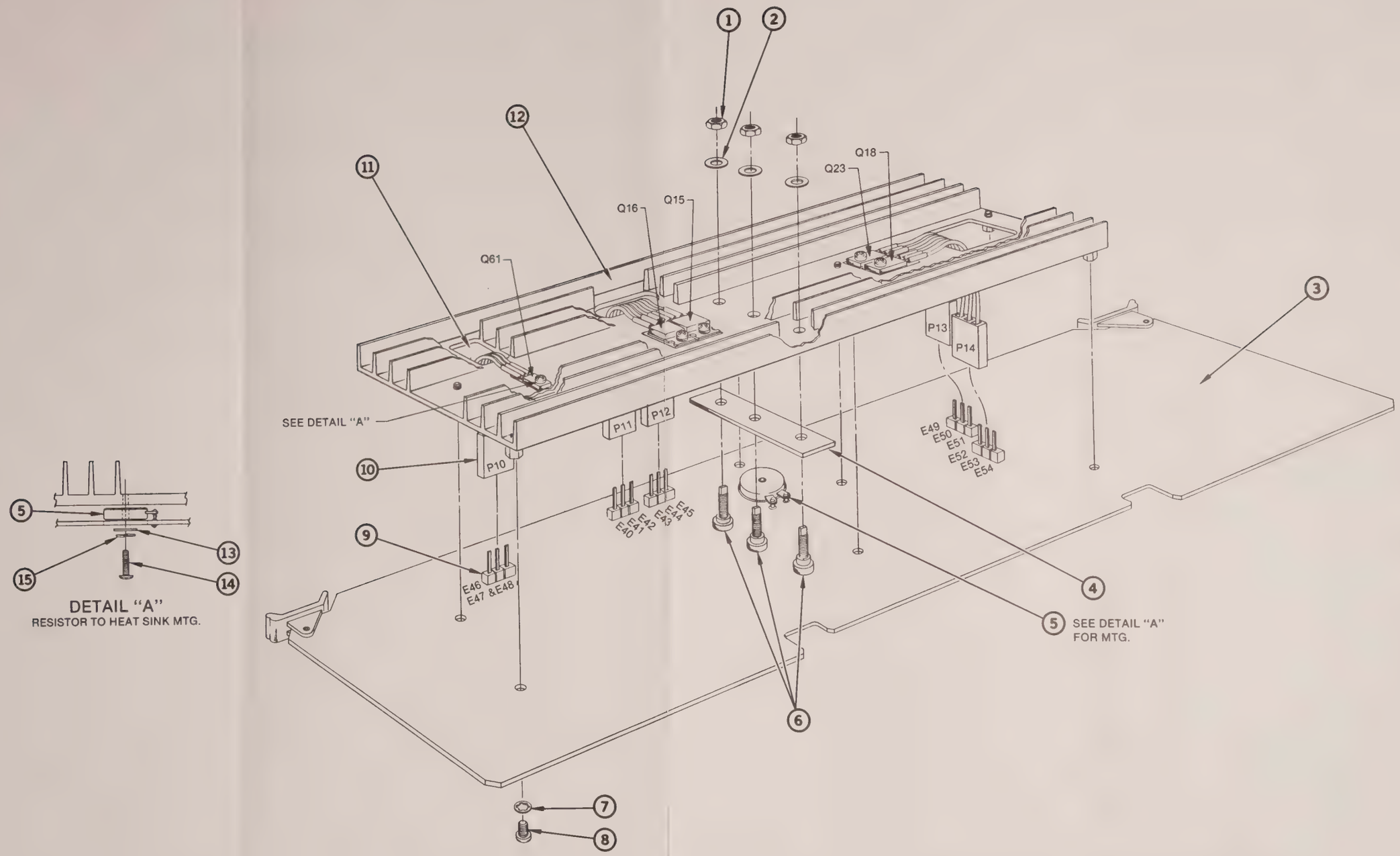


Figure 5-12. Output Amplifier Heat Sink Replacement

REMOVE

1. Remove output amplifier board (3) from chassis (paragraph 5.9.7).
2. Remove 3 nuts (1) and flat washers (2) from heat sink (12).
3. Remove screw (14), lockwasher (15) and flat washer (13) from center of R213 (5).
4. Remove all 5 power transistor connectors (10) from pins (9) on output amplifier board (3).
5. Remove all 7 screws (8) and lockwashers (7) holding heat sink (12) to output amplifier board (3).
6. Carefully lift heat sink (12) away from power amplifier board (3).
7. Lift metal plate (4) away from Q52, Q53 and Q54 (6).

INSTALL

1. Install metal plate (4) on Q52, Q53 and Q54 (6).
2. Coat top of metal plate (4) and top of R213 (5) with thermal compound (Wakefield #120-2).
3. Line up connector pins (9) on foil side of power amplifier board (3) with holes in heat sink (11), then lower heat sink (12) onto board (3).
4. Secure heat sink (12) to power amplifier board (3) with 7 screws (8) and lockwashers (7).
5. Connect all 5 power transistor connectors (10) to pins (9) on power amplifier board (3).
6. Install screw (14), lockwasher (15) and flat washer (13) in center of R213 (5).

CAUTION

For the next step, care must be taken not to overtighten nuts (1) as the transistor (6) solder connections may be fractured.

7. Mount 3 flat washers (2) on heat sink (12) and secure with nuts (1).
8. Insert output amplifier board (3) into chassis (paragraph 5.9.7).
9. Fasten retainer bars (paragraph 5.9.3).
10. Secure top cover to chassis (paragraph 5.9.1).

5.9.21 Output Amplifier Ribbon Assembly

NOTE

Refer to figure 5-13 for this procedure.

REMOVE

1. Remove output amplifier board (1) from chassis (paragraph 5.9.7).

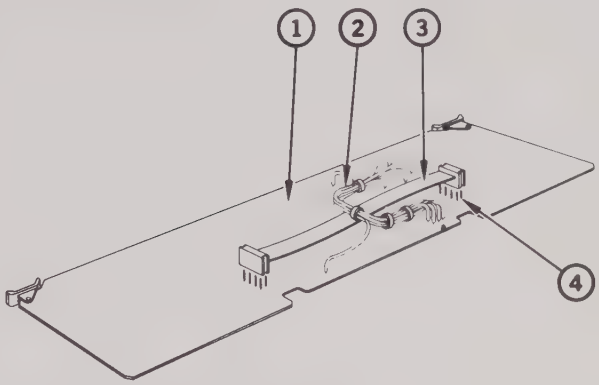


Figure 5-13. Outut Amplifier Ribbon Assembly Replacement

2. Lift wire harness (2) away from ribbon (3) on output amplifier board (1).
3. Disconnect both ends of ribbon (3) from connector pins (4).
4. Feed ribbon (3) through opening under wire harness (2) and remove from board (1).

INSTALL

1. Lift wire harness (2) away from output amplifier board (1).
2. Feed ribbon (3) through opening under wire harness (2).
3. Connect both ends of ribbon (3) to connector pins (4).
4. Push wire harness (2) above ribbon (3) toward output amplifier board (1).
5. Install output amplifier board (1) into chassis (paragraph 5.9.7).
6. Fasten retainer bars (paragraph 5.9.3).
7. Secure top cover to chassis (paragraph 5.9.1).

5.9.22 TIP Packaged Semiconductors

NOTE

Refer to figure 5-14 for this procedure.

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all capacitors to ground to prevent electrical shock.

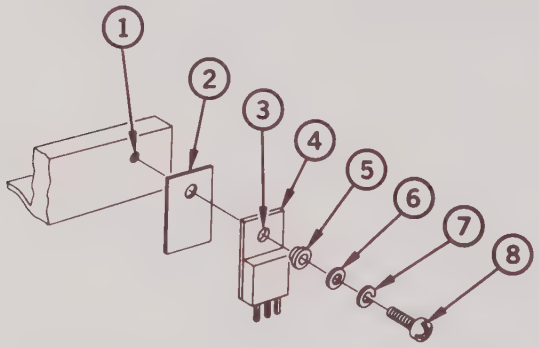


Figure 5-14. TIP Packaged Semiconductor Replacement

NOTE

This task is the same for all TIP packaged semiconductors.

REMOVE

1. Remove mounting screw (8), lock washer (7) and shoulder washer (5) from voltage regulator (4).
2. Remove voltage regulator (4) and insulator (2) from heatsink (1).

INSTALL

1. Coat insulator (2) and back of voltage regulator (4) with thermal compound (Wakefield #120-2).

CAUTION

In the following step, ensure that the shoulder washer (5) fits properly into the voltage regulator hole (3) to prevent shorting the regulator to ground.

2. Thread mounting screw (8) through lock washer (7), shoulder washer (5), voltage regulator (3) and insulator (2), then screw into heatsink (1).

5.9.23 Power Transistors Q2 AND Q6

NOTE

Refer to figure 5-15 for this procedure.

WARNING

Capacitors hold electrical charges after power is removed. Before working on equipment, discharge all capacitors to ground to prevent electrical shock.

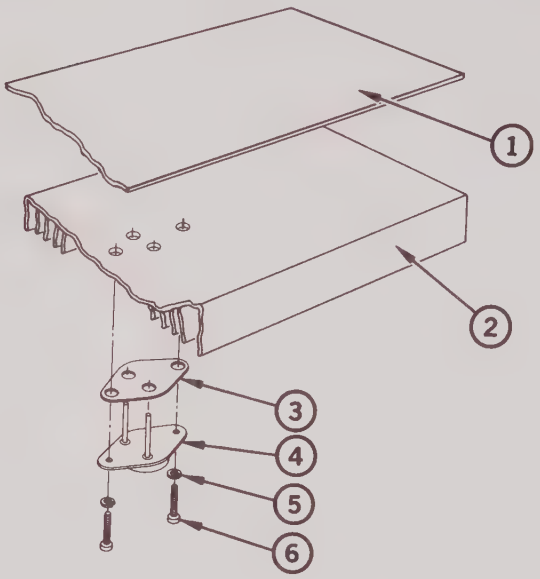


Figure 5-15. Power Transistor Replacement

NOTE

This task is the same for transistors Q2 and Q6. Only Q2 is shown.

REMOVE

1. Remove HI AMP power supply board (1) from chassis (paragraph 5.9.6).
2. Remove 2 mounting screws (6) and lock washers (5) securing Q2 (4).
3. Remove power transistor Q2 (4) and insulator (3) from heatsink (2).

INSTALL

1. Coat insulator (3) and back of 2N5883 power transistor Q2 (4) with thermal compound (Wakefield #120-2).
2. Secure Q2 (4) and insulator (3) to heatsink (2) with 2 mounting screws (6) and lock washers (5).
3. Install HI AMP power supply board (1) in chassis (paragraph 5.9.6).
4. Install LO AMP power supply board in chassis (paragraph 5.9.7).
5. Fasten retainer bars (paragraph 5.9.3).
6. Secure top cover to chassis (paragraph 5.5.1).

5.9.24 Dual Inline Integrated Circuits In Sockets

NOTE

Refer to figure 5-16 for this procedure.

REMOVE

1. Remove top cover (paragraph 5.9.1).
2. Remove appropriate board (paragraph 5.9.7).

NOTE

This task is the same for all dual inline integrated circuits in sockets (8, 14, and 16 pin) on all boards.

3. Using an integrated circuit removal tool, lift the dual inline integrated circuit (1) out of socket (4).

INSTALL

CAUTION

Dot and/or notch (8) on integrated circuit (1) shows the correct position for installation. Install the integrated circuit (1) with dot or notch (8) at similiar notch in drawing (5) on the printed circuit board (7) and socket (6).

1. Position dual inline integrated circuit (1) on socket (4) and insert leads (2) into holes (3).
2. Install PC board (7) in chassis (paragraph 5.9.7).
3. Fasten retainer bars (paragraph 5.9.3).
4. Secure top cover to chassis (paragraph 5.9.1).

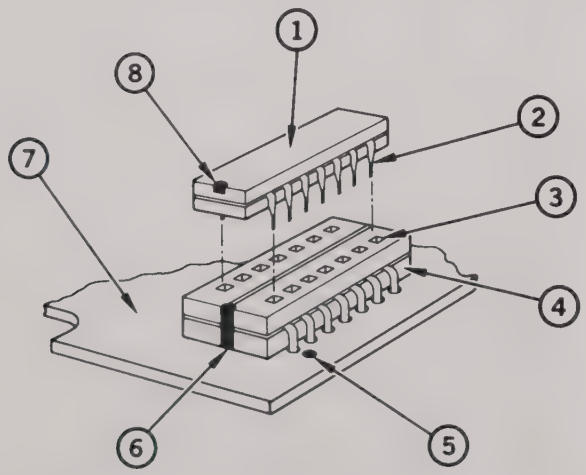


Figure 5-16. Dual Inline IC Replacement

5.9.25 Manual Control Front Panel (With Keyboard and Display)

NOTE

Refer to figure 5-17 for this procedure.

REMOVE

1. Remove top cover (4) from chassis (29) (paragraph 5.9.1).
2. Remove all six screws (34) holding front panel rack mounting brackets (36) to front of chassis (29).
3. Carefully slide front panel (56) away from chassis (29).

NOTE

Do the following steps only if the front panel (56) is to be completely removed.

4. Remove HI AMP power supply board (52) (see paragraph 5.9.6).
5. Remove power switch cable (25) and power light wires (19) from clips (figure 5-4 #14) mounted on inside of chassis (29).
6. Disconnect larger of two connectors (8) from rear panel (13).
7. Remove both Delay and Width boards (26) from chassis (29) (paragraph 5.9.7).
8. Disconnect J20 connector (17) from mother board (39).
9. Remove power switch cable (25) and power light wires (19) from chassis (29).
10. Remove ribbon cable (44) from connector (43) at front of mother board (39).
11. Lift front panel (56) away from chassis (29).

INSTALL

NOTE

If the front panel (56) was not completely removed, begin with step 12.

1. Place front panel (56) near front of chassis (29).
2. Connect ribbon cable (44) to connector (43) at front of mother board (39).
3. Feed power switch cable (25) and power light wires (19) through extreme left of chassis (29).
4. Remove four screws (27) holding rear panel (13) to chassis (29).
5. Slide rear panel (13) back about 1/4 inch and push power light wires (19) under transformer (15) and bracket (16).
6. Connect J20 connector (17) to mother board (39).

7. Being carefull not to pinch any wires, slide rear panel (13) into rear of chassis (29) and secure with 4 screws (27).
8. Install both Delay and Width boards (26) in chassis (29) (paragraph 5.9.7).
9. Connect larger of two connectors (8) to rear panel (13).
10. Slip power switch cable (25) and power light wires (19) into clips (figure 5-4 #14) mounted on inside of chassis (29).
11. Install HI AMP power supply board (52) (paragraph 5.9.6).
12. Carefully slide front panel (56) into front of chassis (29).
13. Secure front panel rack mounting brackets (36) with 6 screws (34).
14. Mount retainer bars (51) (paragraph 5.9.3).
15. Fasten top cover (4) (paragraph 5.9.1).

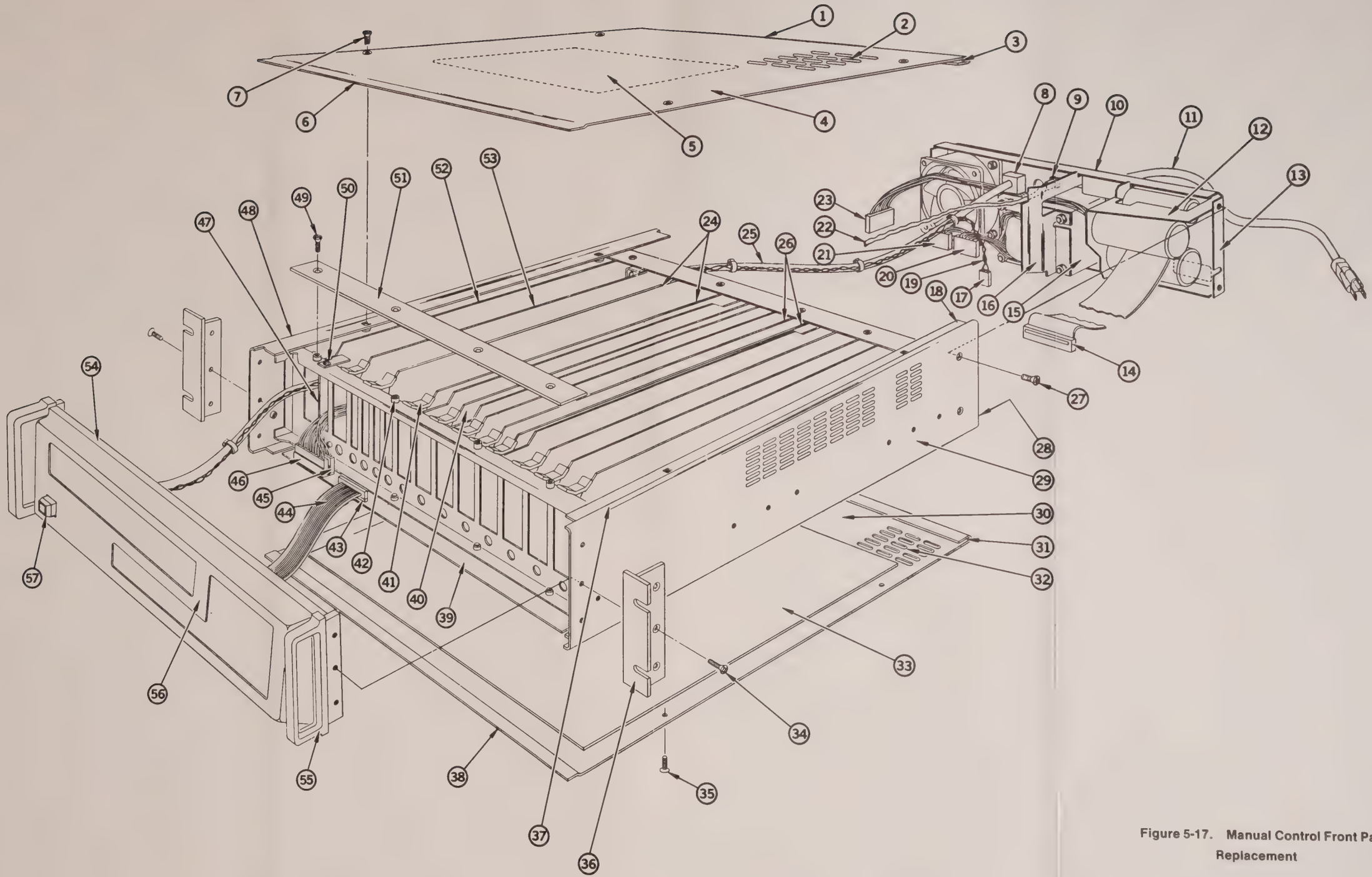


Figure 5-17. Manual Control Front Panel Replacement

Table 5-12. Control Bit Code Definition

(Only item L, Delay Range, is changed.)

L. DELAY RANGE (Address 19, 51)

RANGE	DER5	DER4	DER3	DER2	DER1	DER0
0 - 24 ns	1	1	1	1	1	1
25 ns - 20 μs	1	1	1	1	1	0
20 μs - 100 μs	1	1	1	1	0	0
100 μs - 1 ms	1	1	1	0	0	0
1 ms - 10 ms	1	1	0	0	0	0
10 ms - 100 ms	1	0	0	0	0	0
100 ms - 1.599 s	0	0	0	0	0	0

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown in table 7-1.

7.3. ORDERING PARTS

7.3.1 From Wavetek

When ordering spare parts from Wavetek, please specify part numbers, circuit reference numbers, next high assembly and serial number of the instrument.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly number.

7.3.2 From Other Sources

When ordering components from sources other than Wavetek, use the original manufactures' identifications and part numbers. Table 7-2 gives the full name and FSCMs for the manufactures used in the parts lists.

Table 7-1. Assemblies, Parts Lists and Schematics

Drawing	Drawing Number
Instrument Schematic	0004-00-0249
Chassis Assembly	0102-00-1266
Chassis Parts List	1101-00-1266
Front Panel Assembly	0102-00-1264
Front Panel Parts List	1101-00-1264
Rear Panel Assembly	0102-00-1265
Rear Panel Parts List	1101-00-1265
Mother Board Schematic*	0103-00-0702
Mother Board Assembly*	0101-00-0702
Mother Board Parts List*	1100-00-0702
Hi Amp (Current) Power Supply Schematic*	0103-00-0701
Hi Amp (Current) Power Supply Assembly*	1100-00-0701
Hi Amp (Current) Power Supply Board Assembly*	0101-00-0701
Hi Amp (Current) Power Supply Parts List*	1100-00-0701
Lo Amp (Current) Power Supply Schematic*	0103-00-0700
Lo Amp (Current) Power Supply Assembly*	0101-00-0700
Lo Amp (Current) Power Supply Parts List*	1100-00-0700

*Unchanged drawing. May be found in standard 859 manual.

Table 7-1. Assemblies, Parts Lists and Schematics (Continued)

Drawing	Drawing Number
Output Amplifier Schematic*	0103-00-0698
Output Amplifier Assembly*	1100-00-0698
Output Amplifier Board Assembly*	0101-00-0698
Output Amplifier Parts List*	1100-00-0698
Piggyback Module Assembly*	1208-00-1133
Piggyback Module Parts List*	1208-00-1133
Clock Oscillator Schematic*	0103-00-0693
Clock Oscillator Assembly*	1100-00-0693
Clock Oscillator Parts List*	1100-00-0693
Trigger and Burst Counter Schematic	0103-00-1262
Trigger and Burst Counter Assembly	1100-00-1262
Trigger and Burst Counter Parts List	1100-00-1262
Delay and Width Schematic	0103-00-1260
Delay and Width Assembly	1100-00-1260
Delay and Width Parts List	1100-00-1260
Delay and Width Piggyback Assembly*	1208-00-0697
Delay and Width Piggyback Parts List*	1208-00-0697
Delay Assembly*	0101-00-0697
Scratch Pad Schematic	0103-00-1261
Scratch Pad Assembly	1100-00-1261
Scratch Pad Parts List	1100-00-1261
Microprocessor Schematic	0103-00-1263
Microprocessor Assembly	1100-00-1263
Microprocessor Parts List	1100-00-1263
PROM Package Parts List	1109-00-0018
Selected Set Assembly	1205-00-1322
GPIB Interface Schematic*	0103-00-0685
GPIB Interface Assembly*	0101-00-0685
GPIB Interface Parts List*	1100-00-0685
GPIB Address Assembly*	0101-00-0730
GPIB Address Parts List*	1208-00-0730

*Unchanged drawing. May be found in standard 859 manual.

Table 7-2. Component Manufacturers

Abbreviation	Company	FSCM/Address
3M	Minn. Mining & Mfg.	3M Center Street Paul, Minn. 55144
AB	Allen-Bradley	01121
ACCUR	Accurate Products	93106
AD	Analog Devices	24355
AMP	AMP Incorporated	00779
AMPRX	Amperex Corporation	25403
AMPH	Amphenol Products	02660
AMTOM	Amatom	446 Blake Street New Haven, CT 06515
ANDEV	Analog Devices	24355
A/P	A P Products Incorporated	63878
ARCO	Arco Electronics Incorporated	84171
ARTWR	Artwire	9 Wing Drive Cedar Knolls, NJ 07927
ASHVL	Ashville Schoonmaker	900 Jefferson Avenue Newport News, VA 23607
AVX	AVX Corporation	04222
BECK	Beckman Instruments	80740
BELDN	Beldon Wire & Cable	Box 1980 Richmond, IN 47374
BOURN	Bourns	32999
BRADY	Brady and Associates	62619
BRDRX	Brand Rex Company	07547
BURND	Burndy	00761
CA	Circuit Assembly Corporation	52072
CADDO	Caddock Electronics	19647
CALMK	Calmark Corporation	52094
CAMB	Cambion	1 Alewife Place Cambridge, MA 02140
CAPAR	Capar Components	62462
CARTR	Carter Mfg. Corporation	03929
CDE	Cornell-Dublier	88124
CINCH	Cinch Jones	86168
CORCM	Corcom Incorporated	05245
CORNG	Corning Electronics	28363
CRL	Centralab	99942
DALE	Dale Electronics	91637
DILCO	Dialight	72619
DUNCN	Duncan Electronics	11534
EECO	EECO Incorporated	97525
ELMWD	Elmwood Sensors	14604
ELPAC	Elpac Electronics Incorporated	02980
FAIR	Fairchild Semiconductor	17803
FARIT	FAIR-RITE Products Corporation	34899
FERCO	Ferrite Control Company	1105 Industrial Parkway Brick, NJ 08724
FERRX	Ferroxcube	5083 Kings Highway Saugertus, NY 12477
GE	General Electric Company	06804

Table 7-2. Component Manufacturers (Continued)

Abbreviation	Company	FSCM/Address
GRAHL	Grayhill Incorporated	81073
HI-G	High-G Incorporated	02289
HIT	Hitachi America, Ltd.	62786
HP	Hewlett Packard	28480
HTACH	Hitachi of America	61485
ILSCO	ILSCO	74829
IMC	IMC	08823
INTEL	INTEL Corporation	34649
INTSL	INTERSIL	32293
IR	International Rectifier	59993
ITT	Itt Component	05292
JUDD	Judd Wire	12703
KING	Kings Electronic Company	19212
KINGS	Kings Electronic Company	19212
KSW	KSW	52673
LITFU	Littlefuse	800 E. Northwest Highway Des Plains, IL 60016
MAL	Mallory Capacitor	90201
MCEL	Magnetic Circuit Elements, Inc.	09349
MEPCO	Mepco-Electra	80031
METRS	Milton Ross	511 Second Street Pike Southampton, PA 18966
MICRO	Micro Plastics Incorporated	13764
MOLEX	Molex Connector Corporation	27264
MOT	Motorola	04713
NAT	National Semiconductor	27014
NSC	National Semiconductor	27014
NYGLS	NY Glass	11783
PAMOT	Pamotor	23936
PEM	Pem Eng. & Manuf. Corporation	29743
PHLDG	Phelps Dodge	09040
RCA	RCA	02735
ROBNU	Robinson/Nugent Incorporated	06776
ROYAL	Royal Industries	4250 Morena Boulevard San Diego, CA 92117
SESTM	Seastrom	86928
SIG	Signetics Corporation	18324
SILX	Siliconix, Incorporated	17856
SLCON	Siliconix	17856
SMITH	H.H. Smith	8112 Snediker Street Brooklyn, NY 11207
SOTCO	Southco Incorporated	94222
SPECT	Spectrol	02111
SPRAG	Sprague Electronics	56289
STKPL	Stackpole	78488
STM	Cornell-Dublier (replacement)	Wayne Plaza Wayne, NY 07470
TEKA	Teka Products	45 Salem Street Providence, RI 02907
THERM	Thermalloy	13103

Table 7-2. Component Manufacturers (Continued)

Abbreviation	Company	FSCM/Address
TI	Texas Instruments	33809
TRIKO	Trico	78801
TRW	TRW Capacitors	59792
UNICP	Unicorp	04729
USECO	Useco	15849
WVTK	Wavetek	23338
ZIER	Zierick Mfg. Corporation	79963

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

CHANNEL 1 OUTPUT 20V .4A 50Ω — J23

CHANNEL 2 OUTPUT 20V .4A 50Ω — J24

J28 (CORCOM) — F1 — E29 — R P S L GND B H

J11 P11 (1 2 3 6 7) — J13 P13 (1 2)

DIGITAL GND, DIGITAL GND, +5V UNREG, +5V UNREG, NC, NC, -5.2V UNREG, -5.2V UNREG

P12 J12 — E33 E34 THERMAL SWITCH

POWER SUPPLY HI AMP (A11)

J27 TRIG IN ±10V MAX 1KΩ

J26 SYNC OUT 3V 50Ω

J25 CLOCK OUT 3V 50Ω

REAR PANEL (A2)
1101-00-0672

S2 GPIB ADDRESS SELECTOR — P22

GPIB — J21

DIGITAL GND, UNR +5/1, F15-RT/1, UNR -15/1, UNR -15/2, F15-RT/2, UNR 30H/2, UNR 30L/2, UNR 30H/1, UNR 30L/1, UNR -30SH, UNR -30SL, F15-RT/2, UNR +15V, UNR -15V, SHIELD, DIGITAL GND, DIGITAL GND

P14 J14 — P15 J15 — P19 J19

J1, J1, J2, J3, J4

SCRATCH PAD (A5) — MICRO PROC (A14) — GPIB (A13)

P32 CH1 CH2
P33 CH1 CH2
P34 CH1 CH2
P35 CH1 CH2

J10 POWER SUPPLY LO AMP (A10) — J9 — J8 — J7 CLOCK OSC (A7) — J6 — J5 DELAY/WIDTH CH.1 (A8) — J4 DELAY/WIDTH CH.2 (A15)

OUTPUT AMP CH.2 (A16) — OUTPUT AMP CH.1 (A9) — BURST BD. (A4)

MOTHER BOARD (A12)

J3 — J2 — J1

P16 J16 — J17 P17 — J18 — J20 P20 (3 2 1)

E24	LOW SEN
E3	-2V SEN
E11	-5V SEN
E26	+5V SEN
E1	-2V
E5	-5.2V
E6	-5.2V
E18	+5V
E19	+5V
N.C.	A6
E25	LOW SEN
E4	-2V SEN
E12	-5V SEN
E9	+15V IN
E2	-2V
E7	-5.2V
E8	-5.2V
E16	+5V
E17	+5V
E10	-15V IN

-15V, +15V — R1 100 OHM — DS1

CHASSIS (A3)
1101-00-0670

FRONT PANEL (A1)
1101-00-0

2 3 1 4 7 — S1 POWER SWITCH

ASSEMBLY REF DES

FRONT PANEL	A1
REAR PANEL	A2
CHASSIS	A3
BURST	A4
SCRATCH	A5
CLOCK	A7
W&D	A8
OUTPUT AMP	A9
LO AMP	A10
HI AMP	A11
MOTHER	A12
GPIB	A13
MPROC	A14
W&D	A15
OUTPUT AMP	A16

2ND CHANNEL

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. CHERMACK DATE 1-26-84
PROJ ENGR
RELEASE APPROV 2-28-84
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 XX : 030 ANGLES ±1°
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

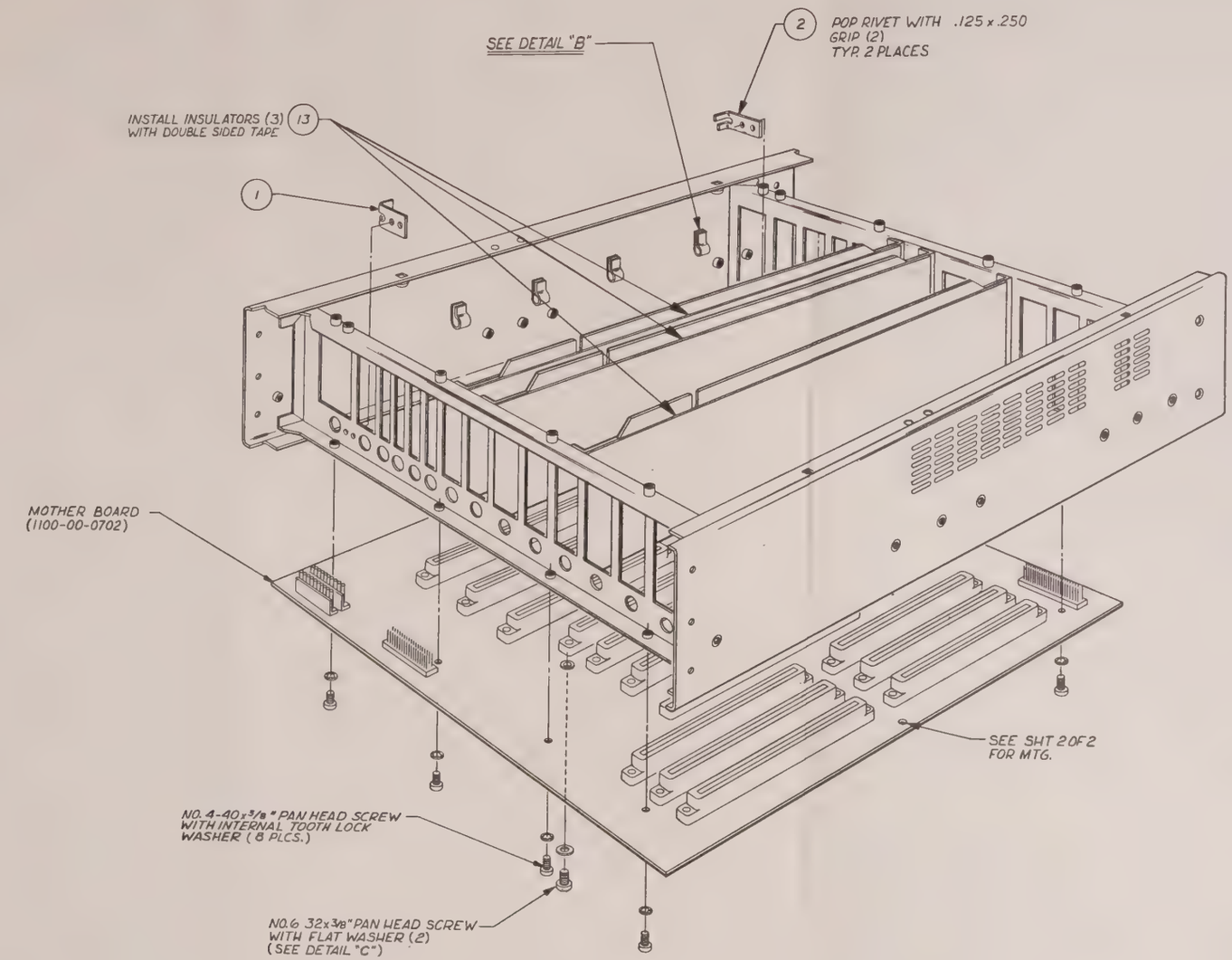
TITLE
SCHEMATIC: INSTRUMENT

MODEL NO 0545402 — DWG NO 1100CC-0249 — REV
CODE IDENT 23338 — SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDED NO. A-3004

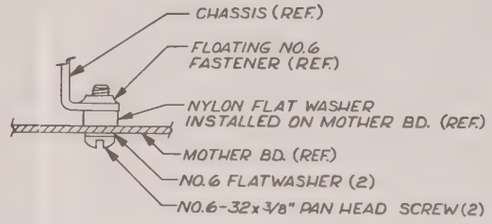
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP


SEE DETAIL "B"
2 POP RIVET WITH .125 x .250 GRIP (2) TYP. 2 PLACES
INSTALL INSULATORS (3) 13 WITH DOUBLE SIDED TAPE
1
MOTHER BOARD (1100-00-0702)
SEE SHT 2 OF 2 FOR MTG.
NO. 4-40 x 5/8" PAN HEAD SCREW WITH INTERNAL TOOTH LOCK WASHER (8 PLCS.)
NO. 6 32x3/8" PAN HEAD SCREW WITH FLAT WASHER (2) (SEE DETAIL "C")

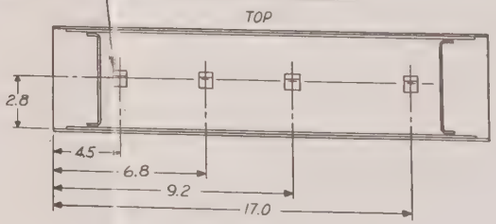
DETAIL "C"

MOTHER BD. HARDWARE STACK-UP (TYP. 2 PLACES ONLY)


CHASSIS (REF.)
FLOATING NO. 6 FASTENER (REF.)
NYLON FLAT WASHER INSTALLED ON MOTHER BD. (REF.)
MOTHER BD. (REF.)
NO. 6 FLATWASHER (2)
NO. 6-32 x 3/8" PAN HEAD SCREW (2)

LOCATE WIRE MOUNTS (4) 10 AS SHOWN

DETAIL "B"
WIRE MOUNT LOCATION



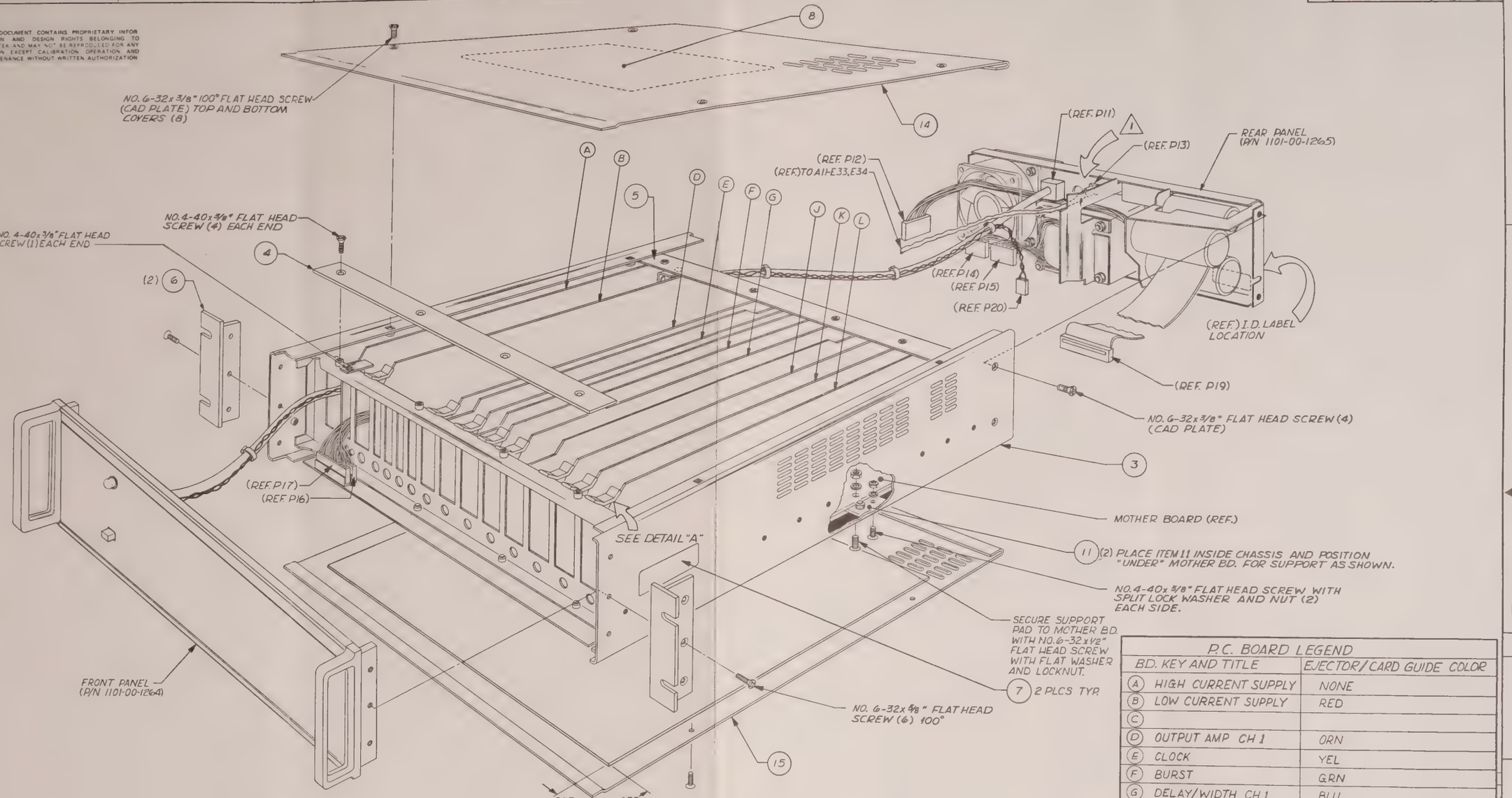
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-2004	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: ASSEMBLY CHASSIS (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 1100 SERIES
	SCALE		DWG NO 0102-00-1266 REV
			CODE IDENT 23338 SHEET 1 OF 3

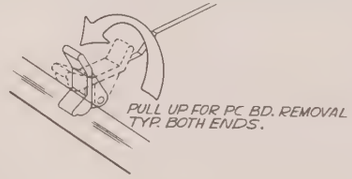
©1990 BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-1394

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP


8
NO. 6-32 x 3/8" 100° FLAT HEAD SCREW (CAD PLATE) TOP AND BOTTOM COVERS (8)
14
(REF. P11)
1
(REF. P13)
REAR PANEL (P/N 1101-00-1265)
(REF. P12)
(REF.) TO A1-E33, E34
A
B
5
D
E
F
G
J
K
L
NO. 4-40 x 3/8" FLAT HEAD SCREW (4) EACH END
NO. 4-40 x 3/8" FLAT HEAD SCREW (1) EACH END
4
(2) 6
(REF. P14)
(REF. P15)
(REF. P20)
(REF.) I.D. LABEL LOCATION
(REF. P19)
NO. 6-32 x 3/8" FLAT HEAD SCREW (4) (CAD PLATE)
3
(REF. P17)
(REF. P16)
SEE DETAIL "A"
MOTHER BOARD (REF.)
11 (2) PLACE ITEM 11 INSIDE CHASSIS AND POSITION "UNDER" MOTHER BD. FOR SUPPORT AS SHOWN.
NO. 4-40 x 3/8" FLAT HEAD SCREW WITH SPLIT LOCK WASHER AND NUT (2) EACH SIDE.
SECURE SUPPORT PAD TO MOTHER BD. WITH NO. 6-32 x 1/2" FLAT HEAD SCREW WITH FLAT WASHER AND LOCKNUT.
7 2 PLCS TYP.
FRONT PANEL (P/N 1101-00-1264)
NO. 6-32 x 5/8" FLAT HEAD SCREW (6) 100°
15
.563
.875
12 PLACE SHIELD ON BOTTOM COVER WITH DOUBLE SIDED TAPE IN SAME POSITION AS MOTHER BD. APPROX. AS SHOWN.

DETAIL "A"
TYP. PC BD. REMOVAL



1 REAR PANEL BNC DESTINATION

PANEL FUNCTION	PC. BD. DESTINATION
J27 "TRIG IN"	A4-J4 BURST BD.
J26 "SYNC OUT"	A4-J3 BURST BD.
J25 "CLOCK OUT"	A4-J2 BURST BD.
J23 "CH.1 OUTPUT"	A9-J1 CH.1 OUTPUT AMP.
J24 "CH.2 OUTPUT"	A16-J1 CH.2 OUTPUT AMP.

NOTE UNLESS OTHERWISE SPECIFIED

P.C. BOARD LEGEND

BD. KEY AND TITLE	EJECTOR/CARD GUIDE COLOR
(A) HIGH CURRENT SUPPLY	NONE
(B) LOW CURRENT SUPPLY	RED
(C)	
(D) OUTPUT AMP CH 1	ORN
(E) CLOCK	YEL
(F) BURST	GRN
(G) DELAY/WIDTH CH 1	BLU
(H)	
(J) GPIB	WHT
(K) MICROPROCESSOR	WHT
(L) RANDOM ACCESS MEMORY	WHT

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN CHERMACK DATE 12-1-83
PROJENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

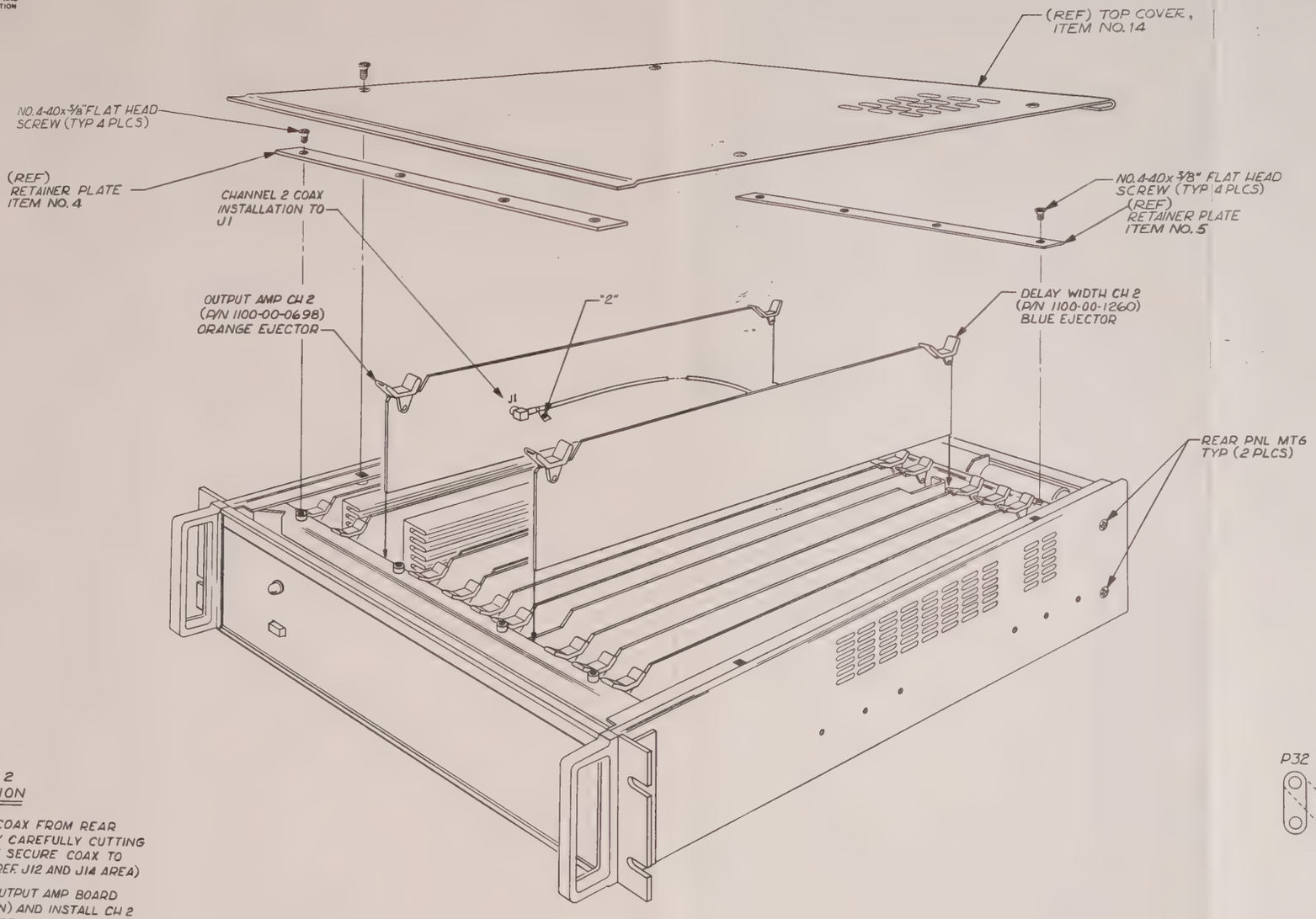
WAVETEK SAN DIEGO, CALIFORNIA

TITLE
ASSEMBLY CHASSIS

MODEL NO 655 5902
DWG NO 0102-00-1266
REV
CODE IDENT 23338
SHEET 2 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP


(REF) TOP COVER, ITEM NO. 14
NO. 4-40 x 3/8" FLAT HEAD SCREW (TYP 4 PLCS)
(REF) RETAINER PLATE ITEM NO. 4
CHANNEL 2 COAX INSTALLATION TO J1
NO. 4-40 x 3/8" FLAT HEAD SCREW (TYP 4 PLCS)
(REF) RETAINER PLATE ITEM NO. 5
OUTPUT AMP CH 2 (P/N 1100-00-0698) ORANGE EJECTOR
"2"
J1
DELAY WIDTH CH 2 (P/N 1100-00-1260) BLUE EJECTOR
REAR PNL MT6 TYP (2 PLCS)

DETAIL "A"
CHANNEL 2
JUMPER LOCATION

CHANNEL 2 INSTALLATION

STEP 1: REMOVE CH2 COAX FROM REAR PANEL AREA BY CAREFULLY CUTTING TY-WRAPS THAT SECURE COAX TO WIRE BUNDLES (REF. J12 AND J14 AREA)

STEP 2: LOCATE "J1" ON OUTPUT AMP BOARD (APPROX AS SHOWN) AND INSTALL CH 2 COAX BEING CAREFULL OF COAX ROUTING. (COMPONENT INTERFERANCE)

STEP 3: INSTALL CH 2 "OUTPUT AMP BOARD" (REF. P/N 1100-00-0698)

STEP 4: INSTALL CH2 "DELAY WIDTH BOARD" (REF. P/N 1100-00-0694)

STEP 5: RELOCATE JUMPERS ON MOTHER BD. AS SHOWN IN DETAIL "A"

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERNACK	DATE 1-86	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY, CHASSIS
	RELEASE APPROV	2-28-86	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 8-59-5-902 DWG NO. C102-00-1266 REV
	SCALE		CODE IDENT 23338 SHEET 3 OF 3

BISHOP GRAPHICS/ACCUPRESS RECORDED NO. A-3894

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-1266	WVTK	0102-00-1266	1
13	INSULATOR REF 3200-03-0001	172-6891	WVTK	1400-00-6891	3
11	SUPPORT PAD	859-9173	WVTK	1400-00-9173	2
1	C	859-9323	WVTK	1400-00-9323	1
2	RETAINER, PC, RH	859-9333	WVTK	1400-00-9333	1
7	LABEL, REAR SUPPORT	859-0010	WVTK	1400-01-0010	2
3	CHASSIS	115-1772	CALMK	1400-01-0022	1
8	LABEL, PCA GIUDE	859-0430	WVTK	1400-01-0430	1
14	COVER, TOP	115-1575-94C	CALMK	1400-01-1002	1
15	COVER, BOTTOM	115-1575-93C	CALMK	1400-01-1012	1
12	INSULATOR, MOTHER BD	859-1411	WVTK	1400-01-1411	1
4	RETAINER PLATE	859-2013	WVTK	1400-01-2013	1
5	RETAINER PLATE	859-2023	WVTK	1400-01-2023	1
6	EAR RACKMOUNT, COLOR	904-6782	WVTK	1400-01-6782	2
NONE	GUIDE, BOARD	115-287	CALMK	2100-06-0004	6
NONE	CARD GUIDE, RED	115-287 RED	CALMK	2100-06-0008	2
NONE	CARD GUIDE, ORANGE	115-287 ORANGE	CALMK	2100-06-0009	4

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS	ASSEMBLY NO 1101-00-1266 PAGE 1	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	CARD GUIDE, YELLOW	115-287 YELLOW	CALMK	2100-06-0010	2
NONE	CARD GUIDE, GREEN	115-287 GREEN	CALMK	2100-06-0011	2
NONE	CARD GUIDE, BLUE	115-287 BLUE	CALMK	2100-06-0012	4
10	WIRE MOUNT, ADHESIVE	6025-08-BLK	GRAHL	2800-00-0024	4

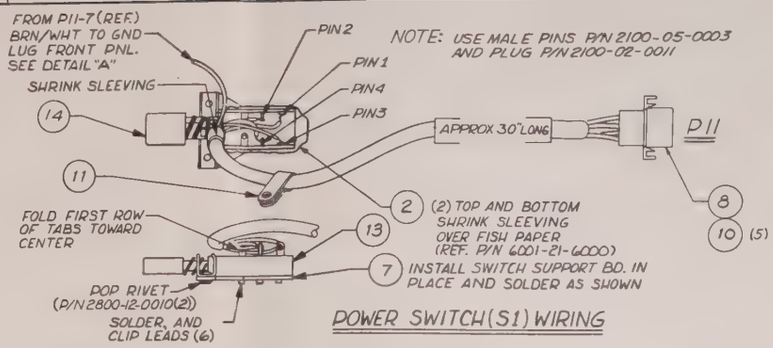
WAVETEK PARTS LIST	TITLE ASSY, CHASSIS	ASSEMBLY NO. 1101-00-1266 PAGE 2	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: CHASSIS ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO. 859-S-902 DWG NO. 1101-00-1266 REV
	SCALE		CAGE IDENT 23338 SHEET 1 OF 1

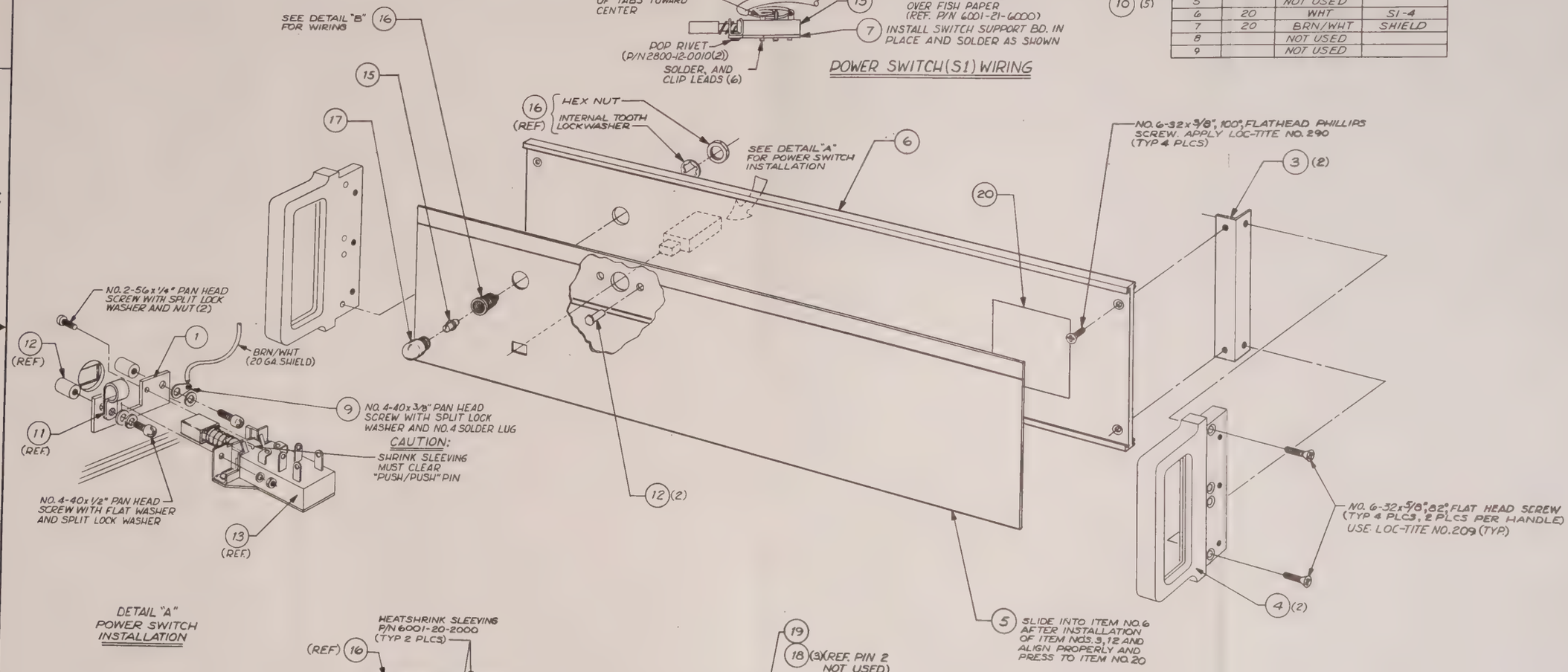
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

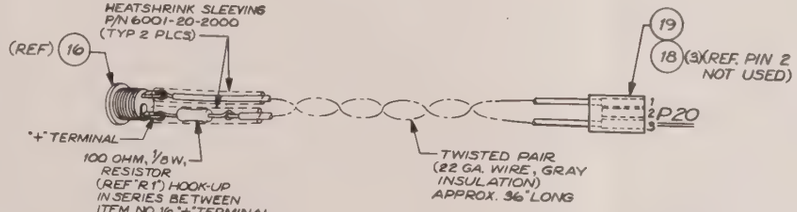


POWER SWITCH (S1) WIRING

P11 WIRE LIST			
PIN NO.	WIRE GA.	COLOR	DESTINATION
1	20	GRN	S1-2
2	20	BLK	S1-3
3	20	RED	S1-1
4		NOT USED	
5		NOT USED	
6	20	WHT	S1-4
7	20	BRN/WHT	SHIELD
8		NOT USED	
9		NOT USED	


SEE DETAIL "B" FOR WIRING
16
15
17
16 (REF) HEX NUT
INTERNAL TOOTH LOCKWASHER
SEE DETAIL "A" FOR POWER SWITCH INSTALLATION
6
20
NO. 6-32 x 3/8", 100° FLATHEAD PHILLIPS SCREW. APPLY LOC-TITE NO. 290 (TYP 4 PLCS)
3 (2)
NO. 2-56 x 1/4" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND NUT (2)
12 (REF)
1
BRN/WHT (20 GA. SHIELD)
9
NO. 4-40 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND NO. 4 SOLDER LUG
11 (REF)
CAUTION: SHRINK SLEEVING MUST CLEAR "PUSH/PUSH" PIN
NO. 4-40 x 1/2" PAN HEAD SCREW WITH FLAT WASHER AND SPLIT LOCK WASHER
13 (REF)
12 (2)
NO. 6-32 x 5/8", 82° FLAT HEAD SCREW (TYP 4 PLCS, 2 PLCS PER HANDLE) USE LOC-TITE NO. 209 (TYP.)
4 (2)
5
SLIDE INTO ITEM NO. 6 AFTER INSTALLATION OF ITEM NOS. 3, 12 AND ALIGN PROPERLY AND PRESS TO ITEM NO. 20

DETAIL "A" POWER SWITCH INSTALLATION


HEATSHRINK SLEEVING P/N 6001-20-2000 (TYP 2 PLCS)
(REF) 16
19
18 (3X) (REF. PIN 2 NOT USED)
P20
"+" TERMINAL
100 OHM, 1/8 W, RESISTOR (REF. "R1") HOOK-UP IN SERIES BETWEEN ITEM NO. 16 "+" TERMINAL AND ITEM NO. 19, PIN NO. 1
TWISTED PAIR (22 GA. WIRE, GRAY INSULATION) APPROX. 36" LONG

DETAIL "B" LAMP ASSEMBLY WIRING

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-23-84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ. ENGR.		TITLE ASSEMBLY FRONT PANEL (A1)
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1°		
	DO NOT SCALE DWG	MODEL NO 859S-902	DWG NO 0102-00-1264 REV
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FRONT PANEL	0102-00-1264	WVTK	0102-00-1264	1
1	BRKT, SWITCH MTG	172-7703	WVTK	1400-00-7703	1
2	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	2
3	BRKT, PANEL SUPPORT	184-1253	WVTK	1400-01-1253	2
4	HANDLE, COLOR FROM: 1400-00-6951	603-6742	WVTK	1400-01-6742	2
5	PANEL, FRONT	859-7690	WVTK	1400-01-7690	1
6	PANEL, SUB	859-7702	WVTK	1400-01-7702	1
20	ADHESIVE	468 3" X 180 FT LONG	3M	1600-02-0013	3
7	SWITCH SUPPORT BD	859-0750	WVTK	1700-00-0750	1
8	PLUG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
19	HEADER, CONN 3 PIN	640440-3	AMP	2100-02-0117	1
18	CABLE CONTACT	226286-2	AMP	2100-03-0040	3
9	SOLDER LUG	11A144	ZIER	2100-04-0025	1
10	PIN, MALE	02-06-2103	MOLEX	2100-05-0003	5
15	LAMP	387	GE	2400-02-0019	1
16	LAMP HOLDER	LH73/1	DILCO	2400-02-0021	1

WAVETEK PARTS LIST	TITLE: ASSY, FRONT PANEL	ASSEMBLY NO.: 1101-00-1264 PAGE: 1	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
17	LENS CAP	LC129T2	DILCO	2400-02-0022	1
11	CABLE CLAMP	535	SMITH	2800-00-0010	1
12	.375H, 4-40 STANDOFF, PRESS	[illegible]-440-12	PEM	2800-06-0014	2
R1	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	1
13	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1
14	BUTTON, BONE GRAY	[illegible]-305	CRL	5103-04-0009	1

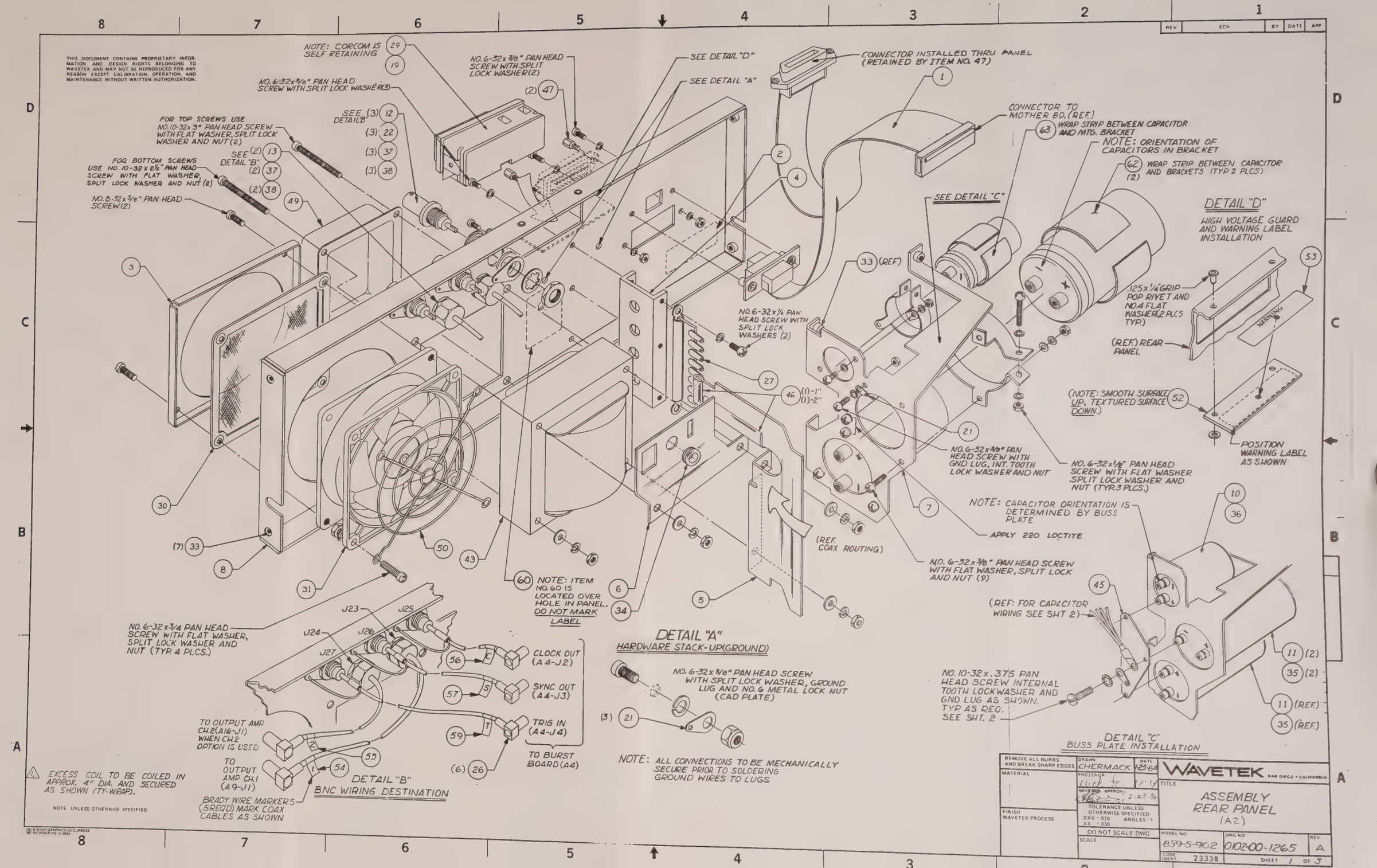
WAVETEK PARTS LIST	TITLE: ASSY, FRONT PANEL	ASSEMBLY NO.: 1101-00-1264 PAGE: 2	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: FRONT PANEL ASSEMBLY
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ±.010 ANGLES ±1, XX ±.030		
	DO NOT SCALE DWG		MODEL NO: 859-S-902 DWG NO: 1101-00-1264 REV
	SCALE		CUST WAVE 23338 SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP


NOTE: CORCOM IS SELF RETAINING
29
19
NO.6-32x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER(2)
(2) 47
NO.6-32x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER(3)
SEE DETAIL "D"
SEE DETAIL "A"
CONNECTOR INSTALLED THRU PANEL (RETAINED BY ITEM NO. 47)
1
CONNECTOR TO MOTHER BD. (REF.)
63 WRAP STRIP BETWEEN CAPACITOR AND MTG. BRACKET
NOTE: ORIENTATION OF CAPACITORS IN BRACKET
62 (2) WRAP STRIP BETWEEN CAPACITOR AND BRACKETS (TYP 2 PLCS)
SEE DETAIL "B" (3) 12 (3) 22 (3) 37 (3) 38
FOR TOP SCREWS USE NO.10-32x 3" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER AND NUT (2)
FOR BOTTOM SCREWS USE NO.10-32x 2 1/2" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER AND NUT (2)
(2) 13 (2) 37 (2) 38
2
4
SEE DETAIL "C"
NO.8-32x3/8" PAN HEAD SCREW(2)
49
3
33 (REF)
DETAIL "D"
HIGH VOLTAGE GUARD AND WARNING LABEL INSTALLATION
53
.125x1/4 GRIP POP RIVET AND NO.4 FLAT WASHER,(2 PLCS TYP.)
WARNING
(REF.) REAR PANEL
NO.6-32x1/4 PAN HEAD SCREW WITH SPLIT LOCK WASHERS (2)
27
46 (1)-1" (1)-2"
(NOTE: SMOOTH SURFACE UP, TEXTURED SURFACE DOWN.) 52
POSITION WARNING LABEL AS SHOWN
21
NO.6-32x3/8" PAN HEAD SCREW WITH GND LUG, INT. TOOTH LOCK WASHER AND NUT
NO.6-32x1/2" PAN HEAD SCREW WITH FLAT WASHER SPLIT LOCK WASHER AND NUT (TYP.3 PLCS.)
30
(7) 33
8
31
50
43
60 NOTE: ITEM NO.60 IS LOCATED OVER HOLE IN PANEL. DO NOT MARK LABEL
6
34
5
(REF. COAX ROUTING)
7
NOTE: CAPACITOR ORIENTATION IS DETERMINED BY BUSS PLATE
APPLY 220 LOCTITE
NO.6-32x3/8" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK AND NUT (9)
10
36
45
(REF: FOR CAPACITOR WIRING SEE SHT 2)
NO.6-32x3/4 PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER AND NUT (TYP. 4 PLCS.)
J23 J25 J24 J26 J27
56 CLOCK OUT (A4-J2)
57 SYNC OUT (A4-J3)
59 TRIG IN (A4-J4)
TO BURST BOARD (A4)
(6) 26
TO OUTPUT AMP CH.2 (A16-J1) WHEN CH.2 OPTION IS USED
TO OUTPUT AMP CH.1 (A9-J1)
55
54
BRADY WIRE MARKERS (5REQD) MARK COAX CABLES AS SHOWN
DETAIL "B"
BNC WIRING DESTINATION
DETAIL "A"
HARDWARE STACK-UP(GROUND)
NO.6-32x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER, GROUND LUG AND NO.6 METAL LOCK NUT (CAD PLATE)
(3) 21
NOTE: ALL CONNECTIONS TO BE MECHANICALLY SECURE PRIOR TO SOLDERING GROUND WIRES TO LUGS
NO.10-32x.375 PAN HEAD SCREW INTERNAL TOOTH LOCKWASHER AND GND LUG AS SHOWN. TYP AS REQ. SEE SHT. 2
11 (2)
35 (2)
11 (REF.)
35 (REF.)
DETAIL "C"
BUSS PLATE INSTALLATION
EXCESS COIL TO BE COILED IN APPROX. 4" DIA. AND SECURED AS SHOWN (TY-WRAP).
NOTE UNLESS OTHERWISE SPECIFIED

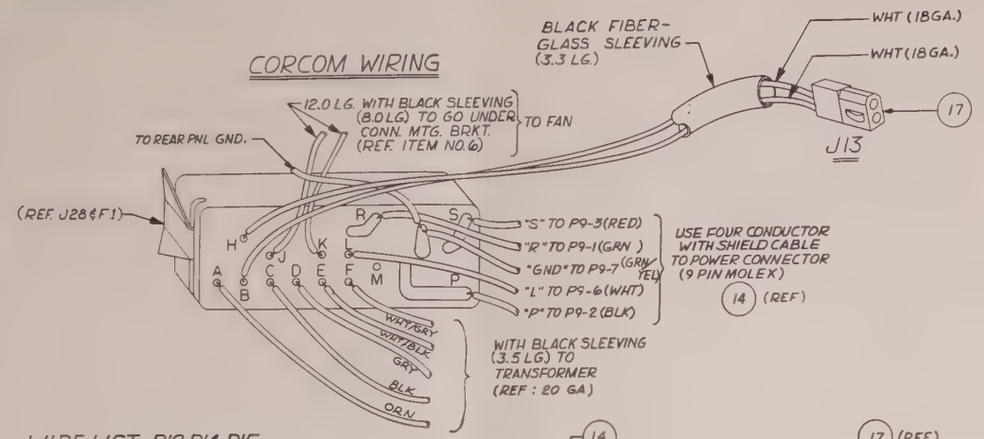
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 12-3-84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE
	MFG ENGR APPROV 2-28-84		ASSEMBLY REAR PANEL (A2)
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 859-5-902	DWG NO 010200-1265 REV A
		CODE IDENT 23338	SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3984

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

CORCOM WIRING


BLACK FIBER-GLASS SLEEVING (3.3 LG.)
WHT (18GA.)
WHT (18GA.)
17
J13
12.0 LG. WITH BLACK SLEEVING (8.0 LG) TO GO UNDER CONN. MTG. BRKT. (REF. ITEM NO. 6)
TO FAN
TO REAR PNL GND.
(REF. J28 & F1)
"S" TO P9-3 (RED)
"R" TO P9-1 (GRN)
"GND" TO P9-7 (GRN/YEL)
"L" TO P9-6 (WHT)
"P" TO P9-2 (BLK)
USE FOUR CONDUCTOR WITH SHIELD CABLE TO POWER CONNECTOR (9 PIN MOLEX)
14 (REF)
WHT/GRY
WHT/BLK
GRY
BLK
ORN
WITH BLACK SLEEVING (3.5 LG) TO TRANSFORMER (REF: 20 GA)

WIRE LIST P12, P14, P15

P12

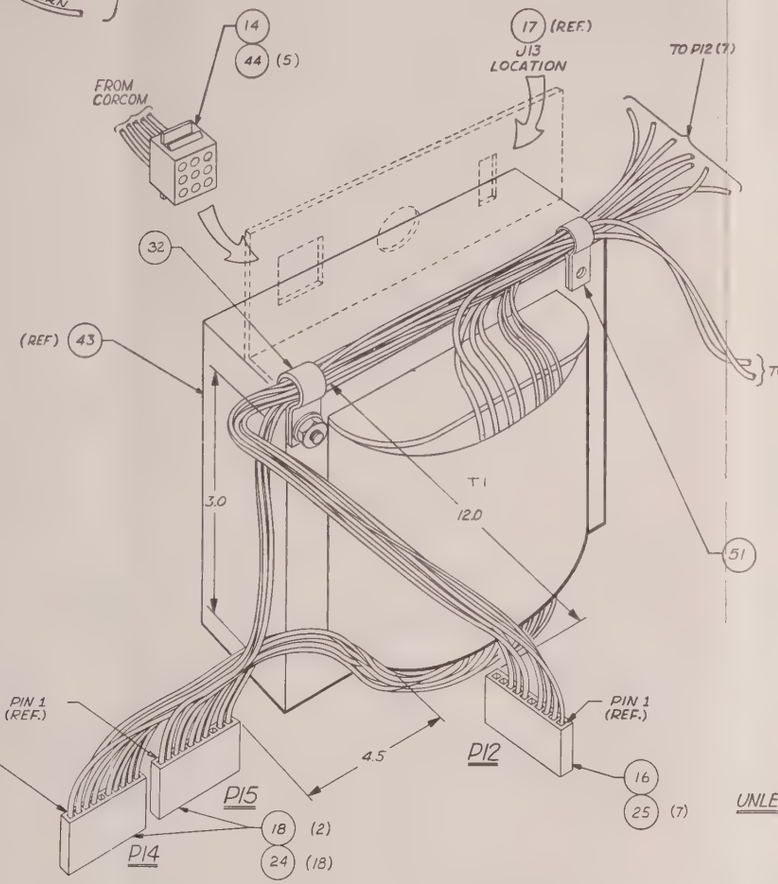
PIN NO.	WIRE GA.	COLOR	FROM	LG.
1	18	WHT	DIGITAL GND.	19.0
2	18	WHT	DIGITAL GND.	19.0
3	18	RED	+5V UNREG.	19.5
4	18	RED	+5V UNREG.	19.5
5			N.C.	
6	18	BLU	-2V UNREG.	18.5
7	18	GRN	-5.2V UNREG.	19.5
8	18	GRN	-5.2V UNREG.	19.5
9			N.C.	
10			N.C.	

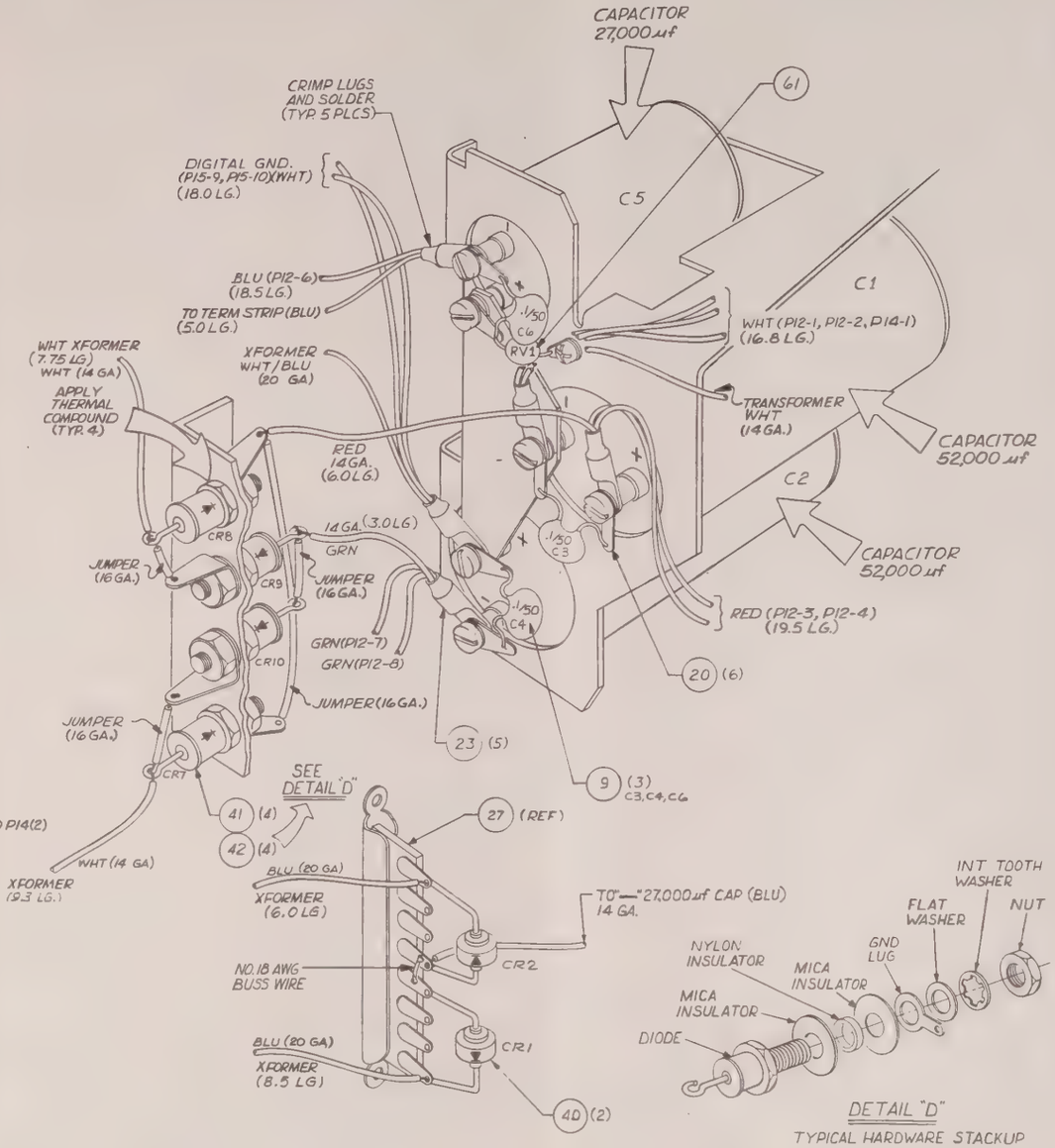
P14

PIN NO.	WIRE GA.	COLOR	FROM	LG.
1	18	WHT	DIGITAL GND.	18
2	24	RED	UNR+15/1	XFORMER
3	24	WHT/RED	F15-RT/1	"
4	24	RED	UNR-15/1	"
5			N.C.	"
6	24	BRN	UNR+15/2	"
7	24	BRN	UNR-15/2	"
8	24	WHT/BRN	F10-RT/2	"
9	20	YEL	UNR+30H/2	"
10	20	YEL	UNR+30L/2	XFORMER

P15

PIN NO.	WIRE GA.	COLOR	FROM	LG.
1	20	WHT	UNR+30H/1	XFORMER
2	20	WHT	UNR+30L/1	"
3	22	WHT/VIO	UNR-15OSH	"
4	22	WHT/VIO	UNR-15OSL	"
5	24	WHT/GRN	UNR±15CT	"
6	24	GRN	UNR+15	"
7	24	GRN	UNR-15	"
8			SHIELD	XFORMER
9	18	WHT	DIGITAL GND.	18.0
10	18	WHT	DIGITAL GND.	18.0





DETAIL "D"
TYPICAL HARDWARE STACKUP

ALL WIRES TO BE 18GA. UNLESS OTHERWISE SPECIFIED.

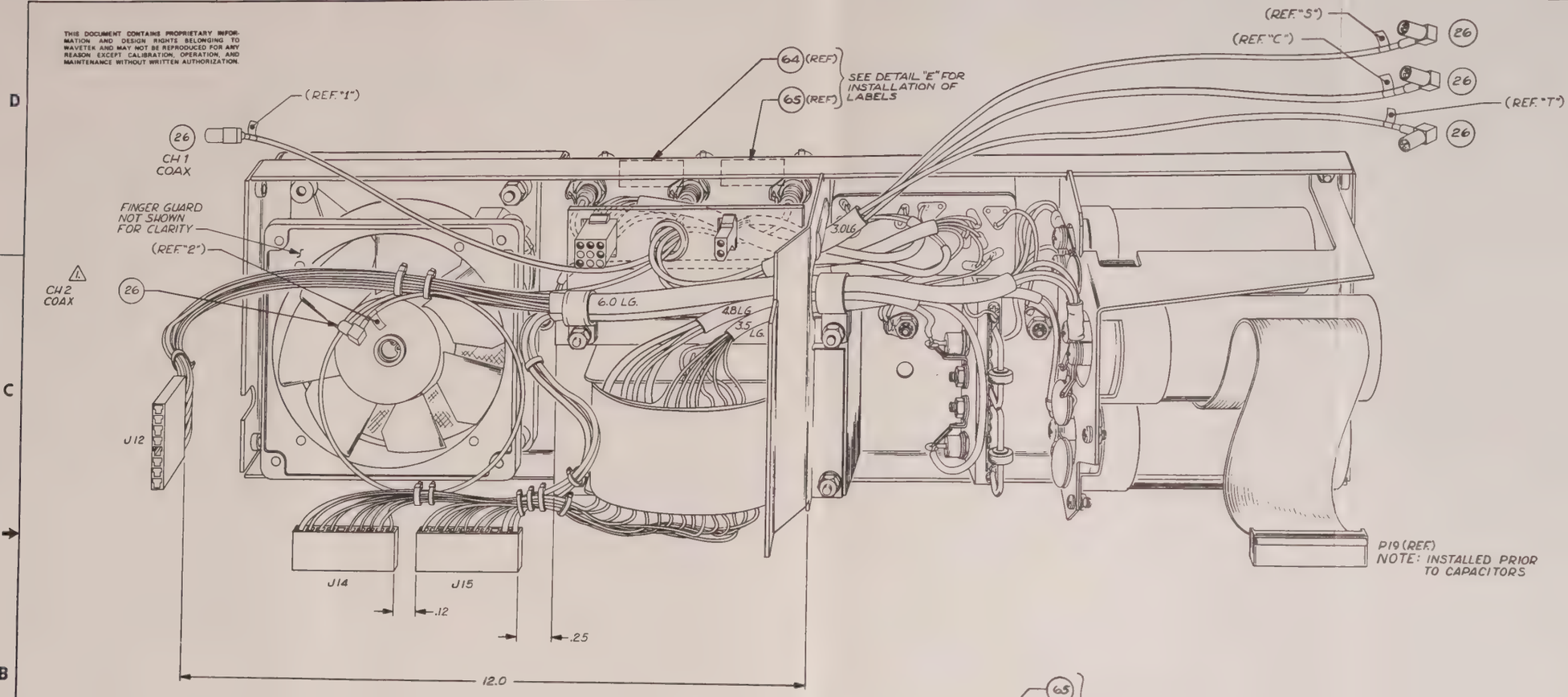
NOTE UNLESS OTHERWISE SPECIFIED

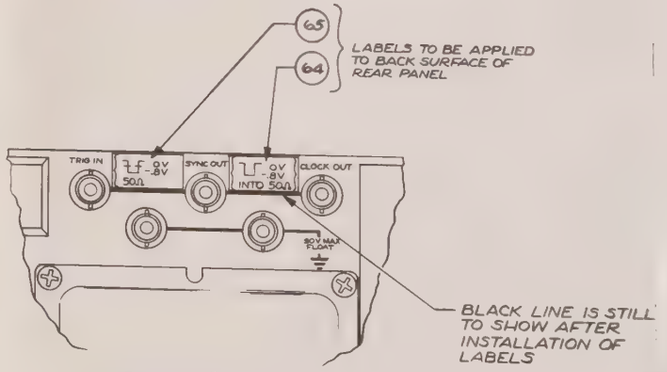
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHRMACK	DATE 1-3-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG SCALE	MODEL NO 8503402	DWG NO 0102-00-1265 REV A
		CODE IDENT 23338	SHEET 2 OF 3

© B-SIZE DRAWN CS ACCUPRESS RECORDER NO. A 3556

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP





DETAIL "E"

REAR PANEL BNC CONNECTORS

P/L ITEM NO	FROM	TO	WIRE	LG.	FUNCTION	MKR.
26	J23	A9-J1	RG174 U	16"	CH1 OUTPUT	1
26	J24	A16-J1	RG174/U	16"	CH2 OUTPUT	2
⚠1 26	J25	A4-J2	RG174/U	33"	CLOCK OUT	C
26	J26	A4-J3	RG174/U	62"	SYNC OUT	S
26	J27	A4-J4	RG174/U	14"	TRIG IN	T

3. COLOR OF PIGTAIL OF COAXES SHOULD REFLECT THEIR LENGTH (PER WAVETEK STANDARDS ASSEMBLY MANUAL.)
2. ALL WIRE LENGTHS ARE APPROX.
⚠1 INSTALL TY-WRAPS AS SHOWN.

NOTE UNLESS OTHERWISE SPECIFIED

© BISHOP GRAPHICS/ACCUMPRESS RECORDS NO. A-3886

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 1-20-84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENG		TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859-5-902	DWG NO 0102-00-1265 REV A
	SCALE	CODE IDENT 23338	SHEET 3 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-1265	WVTK	0102-00-1265	1
NONE	TRANSFORMER	859-0023	WVTK	1204-00-0023	1
1	PCA, GPIB ADDRESS	859-0730	WVTK	1208-00-0730	1
3	SCREEN COVER	172-7523	WVTK	1400-00-7523	1
60	LABEL, OPTION	172-8880	WVTK	1400-00-8880	1
2	I.D. LABEL	801-9090	WVTK	1400-00-9090	1
4	BRACKET, POWER DIODE	859-9253	WVTK	1400-00-9253	1
5	STOP, AIR	859-9263	WVTK	1400-00-9263	1
6	BRACKET, CONN MTG	859-9273	WVTK	1400-00-9273	1
7	BRACKET	859-9283	WVTK	1400-00-9283	1
8	REAR PANEL	859-9290	WVTK	1400-00-9290	1
45	BUSS PLATE	859-0261	WVTK	1400-01-0261	1
NONE	JACK SCREW	859-0530	WVTK	1400-01-0530	2
49	END BELL	859-0574	WVTK	1400-01-0574	1
52	GUARD, HIGH VOLTAGE	859-1391	WVTK	1400-01-1391	1
53	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
62	IPOLYESTER FILM	175-3191	WVTK	1400-01-3191	2

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-1265 | PAGE: 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	REF: 1600-99-0002				
63	REF: 1600-99-0002 POLYESTER FILM SHIELD	859-4791	WVTK	1400-01-4791	1
65	LABLE, BNC TRIG IN	859-7850	WVTK	1400-01-7850	1
64	LABLE, BNC SYNC OUT, CLK OUT	859-7860	WVTK	1400-01-7860	1
9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	3
10	CAP, ELEC, 27000MF, 10V	FAHM27000-10-A2	CDE	1500-32-7301	1
11	CAP, ELEC, 52000MF, 15V	FAHM52000-15-B3	CDE	1500-35-2301	2
12	BNC CONN	U0657/U	AMPH	2100-01-0003	3
13	BNC CONN	KC-19-152	KING	2100-01-0006	2
14	PLUG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
16	CONN HOUSING	1-87025-6	AMP	2100-02-0077	1
17	CONN RECEPTACLE	03-06-1022	MOLEX	2100-02-0083	1
18	CONN HOUSING	09-50-7101	MOLEX	2100-02-0087	2
19	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
20	TERM, LOCK LUG	1414-10	SMITH	2100-04-0007	6
21	TERM, LOCK LUG	1414-6	SMITH	2100-04-0009	3

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-1265 | PAGE: 2 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
22	SOLDER LUG	1497	SMITH	2100-04-0012	3
23	LUG	35	ILSCO	2100-04-0018	5
44	PIN, FEMALE	02-06-1103	MOLEX	2100-05-0002	5
24	PIN	08-50-0105	MOLEX	2100-05-0025	18
25	CONN PINS	87027-3	AMP	2100-05-0047	7
26	CONN	27-843	AMPH	2100-07-0009	5
27	TERMINAL STRIP	3008	SMITH	2100-09-0014	1
29	FUSE, 3A, 250V, S-B	313.003	LITFU	2400-05-0024	1
30	FAN FILTER	3902	PAMOT	2600-01-0005	1
50	FINGER GUARD	65-175	IMC	2600-01-0007	1
31	FAN, MODIFIED FROM: 2600-00-0005	2600-99-0002	WVTK	2600-99-0002	1
NONE	CABLE CLAMP	832	SMITH	2800-00-0009	2
32	CABLE CLAMP	835	SMITH	2800-00-0010	1
51	CABLE CLAMP	840	SMITH	2800-00-0016	1
33	INSERT @ 6	74-11-106-13	SOTCO	2800-09-0017	7
34	GROMMET, RUBBER	2177	SMITH	2800-10-0005	1
35	CAP, MTG, BKT	FJMR	STM	2800-12-0006	2

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-1265 | PAGE: 3 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
36	CAP, MTG, BKT	FHMR-2	STM	2800-12-0007	1
37	WASHER, SHOULDER	2668	SMITH	2800-27-0004	5
38	NYLON FLAT WASHER	2264-N-385	AMTOM	2800-28-0005	5
46	RUBBER SEAL	303	ROYAL	3000-00-0005	1
54	WIRE MARKER "1"	TMM-1	BRADY	3000-00-0076	1
55	WIRE MARKER "2"	TMM-2	BRADY	3000-00-0077	1
56	WIRE MARKER "C"	TMM-C	BRADY	3000-00-0078	1
57	WIRE MARKER "8"	TMM-8	BRADY	3000-00-0079	1
59	WIRE MARKER "T"	TMM-T	BRADY	3000-00-0081	1
61	VARISTOR	V56ZA8	GE	4799-00-0048	1
40	DIODE	MR751	MOT	4801-02-0751	2
41	DIODE	IR30F0030	IR	4899-00-0018	4
42	DIODE, MOUNTING KIT REF: 4899-00-0018	40-8021	IR	4899-00-0019	4

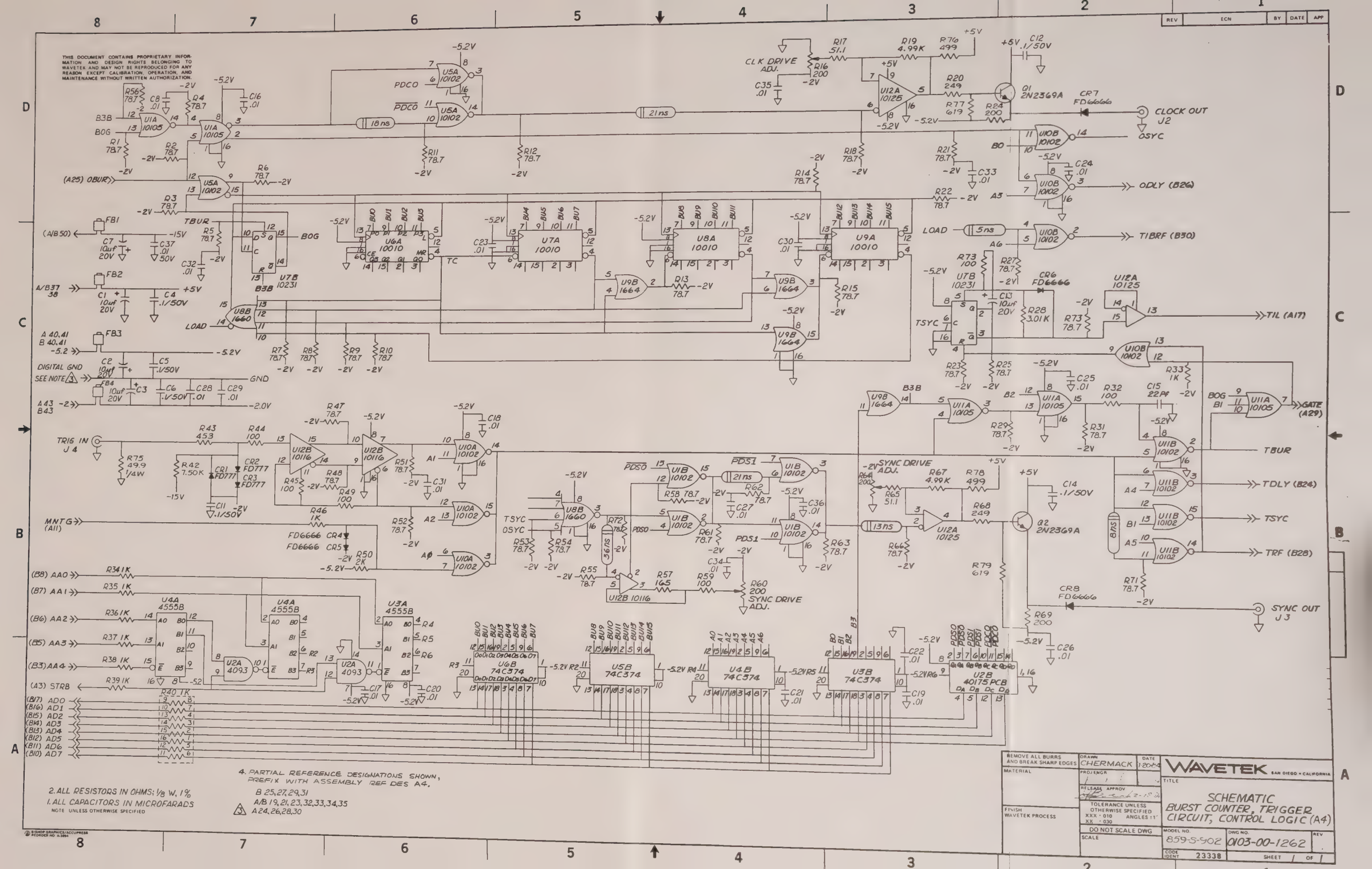
WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-1265 | PAGE: 4 | REV

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: REAR PANEL ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MFG NO: 859-S-902 DWG NO: 1101-00-1265 REV
	SCALE		CAGE CODE: 23338 SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP



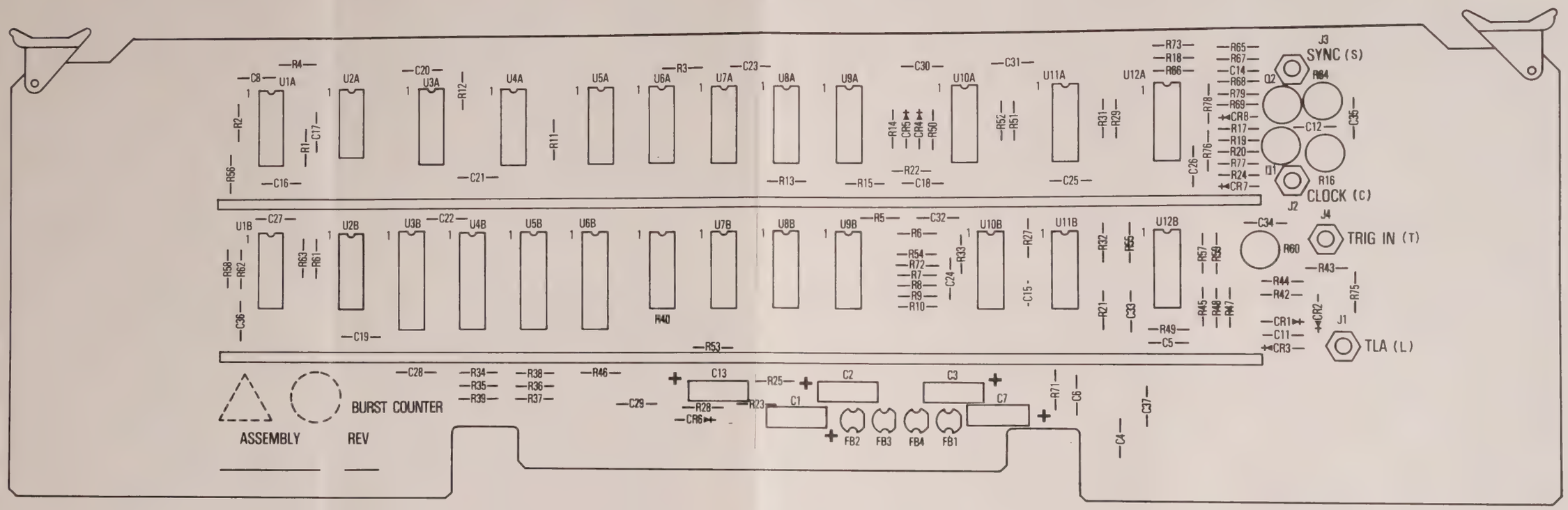
2. ALL RESISTORS IN OHMS; 1/8 W, 1%
1. ALL CAPACITORS IN MICROFARADS
NOTE UNLESS OTHERWISE SPECIFIED

4. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REF DES A4.
B 25,27,29,31
A/B 19,21,23,32,33,34,35
3 A24,26,28,30

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-20-84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
FINISH WAVETEK PROCESS	RELEASE APPROV		SCHEMATIC BURST COUNTER, TRIGGER CIRCUIT, CONTROL LOGIC (A4)
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO. 859-5-902	DWG NO. 0103-00-1262 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: TRIGGER & BURST COUNTER
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 859 / DWG NO 1100-00-1262 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, BURST BOARD	0101-00-1262	WVTK	0101-00-1262	1
NONE	SCHEMATIC, BURST BOARD	0103-00-1262	WVTK	0103-00-1262	1
C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C8	CAP,CER,MN,.01MF,50V	CAC02Z5U103Z100A	CORNO	1500-01-0310	23
C11 C12 C14 C4 C5 C6	CAP,CER,MON,.1MF,50V	CAC03Z5U104Z050A	CORNO	1500-01-0405	6
C15	CAP,CER,22PF,1KV	DD-220	CRL	1500-02-2011	1
C1 C13 C2 C3 C7	CAP,TANT,10MF,20V	150D106X9020B2	SPRAG	1500-71-0601	5
NONE	BURST BOARD	859-0687	WVTK	1700-00-0687	1
J2 J3 J4	CONN	27-848	AMPH	2100-07-0011	3
NONE	PC BD EJECTOR	103 GREEN	CALMK	2800-07-0013	2
NONE	WASHER,FLAT FIBRE #1	5602-4-32	SEBTM	2800-28-0006	4
FB1 FB2 FB3 FB4	BALUN CORE	2873000902	FARIT	3100-00-0002	4
R16 R60 R64	POT,TRIM,200	91AR200	BECK	4600-02-0101	3
R32 R44 R45 R49 R59 R74	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	6
R33 R34 R35 R36 R37	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	8

WAVETEK PARTS LIST | TITLE: ASSY, BURST COUNTER TRIGGER CIRCUIT CONTROL LOGIC BD | ASSEMBLY NO. 1100-00-1262 | PAGE: 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R38 R39 R46					
R57	RES,MF,1/8W,1%,165	RN55D-1650F	TRW	4701-03-1650	1
R24 R69	RES,MF,1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	2
R50	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	1
R20 R68	RES,MF,1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	2
R28	RES,MF,1/8W,1%,3.01K	RN55D-3011F	TRW	4701-03-3011	1
R43	RES,MF,1/8W,1%,453	RN55D-4530	TRW	4701-03-4530	1
R76 R78	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	2
R19 R67	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	2
R17 R65	RES,MF,1/8W,1%,51.1	RN55D-51R1F	TRW	4701-03-5119	2
R77 R79	RES,MF,1/8W,1%,619	RN55D-6190F	TRW	4701-03-6190	2
R42	RES,MF,1/8W,1%,7.5K	RN55D-7501F	TRW	4701-03-7501	1
R1 R10 R11 R12 R13 R14 R15 R18 R2 R21 R22 R23 R25 R27 R29 R3 R31 R4 R47 R48 R5 R51 R52 R53 R54 R55 R56 R58 R6 R61 R62 R63 R66 R7 R71 R72 R73 R8 R9	RES,MF,1/8W,1%,78.7	RN55D-78R7F	TRW	4701-03-7879	39
R75	RES,MF,1/4W,1%,49.9	RN60D-49R9F	TRW	4701-13-4999	1

WAVETEK PARTS LIST | TITLE: ASSY, BURST COUNTER TRIGGER CIRCUIT CONTROL LOGIC BD | ASSEMBLY NO. 1100-00-1262 | PAGE: 2 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R40	RES MODULE	4116R-001-102	BOURN	4770-00-0019	1
CR1 CR2 CR3	DIODE	FD777	FAIR	4807-02-0777	3
CR4 CR5 CR6 CR7 CR8	DIODE	1N4148	FAIR	4807-02-6666	5
Q1 Q2	TRANS	2N2369A	MOT	4901-02-3691	2
NONE	BUSS BAR	6009-90-0009	WVTK	6009-90-0009	2
U8B	IC	MC1660	MOT	8000-16-6000	1
U9B	IC	MC1664	MOT	8000-16-6400	1
U2A	IC	CD4093BE	RCA	8000-40-9300	1
U3A U4A	IC	F4555B	FAIR	8000-45-5500	2
U6A U7A U8A U9A	IC	F10010	FAIR	8001-00-1000	4
U10A U10B U11B U1B U5A	IC	MC10102	MOT	8001-01-0200	5
U11A U1A	IC	MC10105	MOT	8001-01-0500	2
U12B	IC	MC10116P	MOT	8001-01-1600	1
U12A	IC	MC10125P	MOT	8001-01-2500	1
U7B	IC	MC10231	MOT	8001-02-3100	1
U2B	IC	40175	NAT	8004-01-7500	1
U3B U4B U5B U6B	IC	74C374	NAT	8007-43-7430	4

WAVETEK PARTS LIST | TITLE: ASSY, BURST COUNTER TRIGGER CIRCUIT CONTROL LOGIC BD | ASSEMBLY NO. 1100-00-1262 | PAGE: 3 | REV

NOTE UNLESS OTHERWISE SPECIFIED

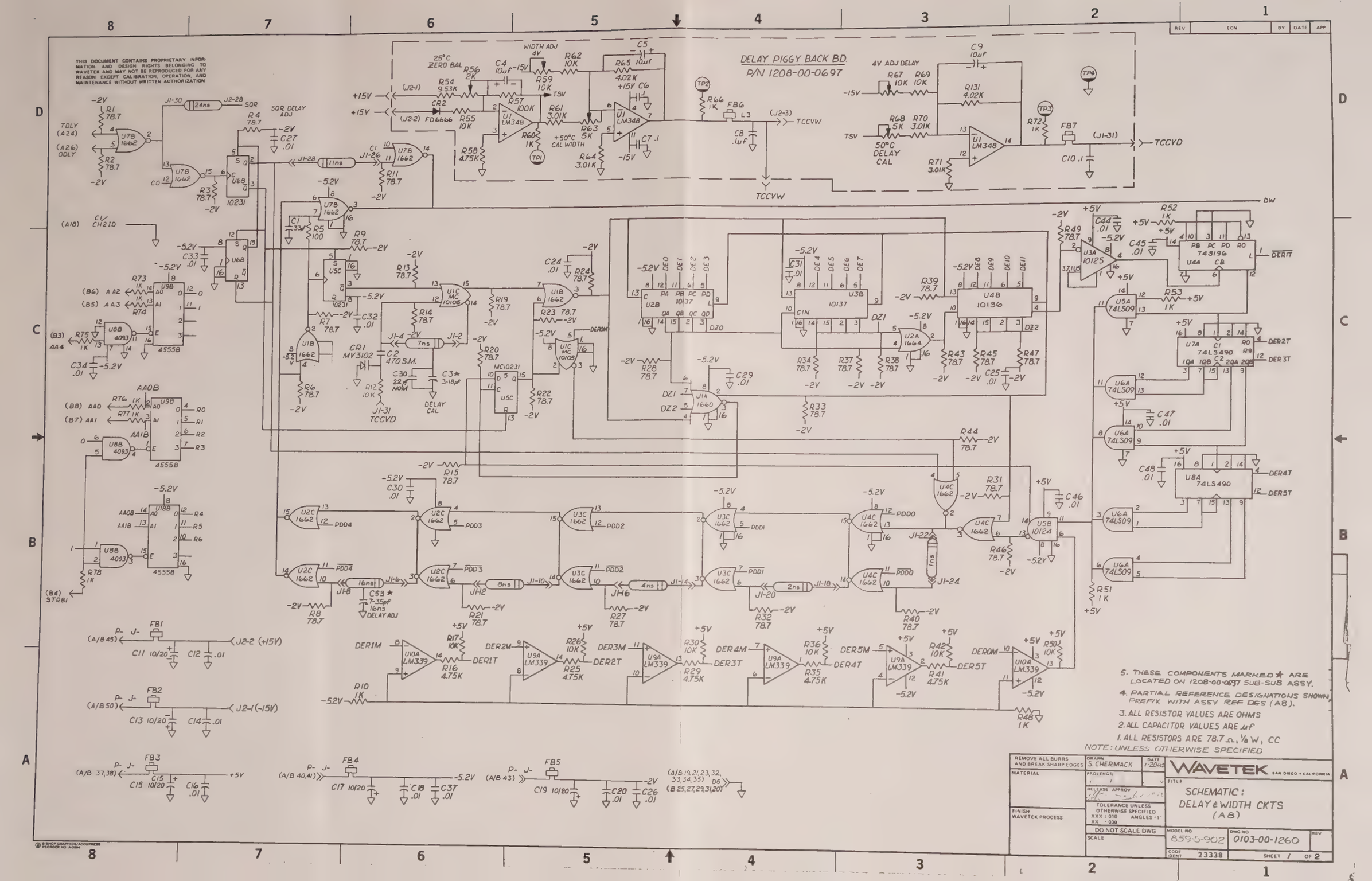
REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

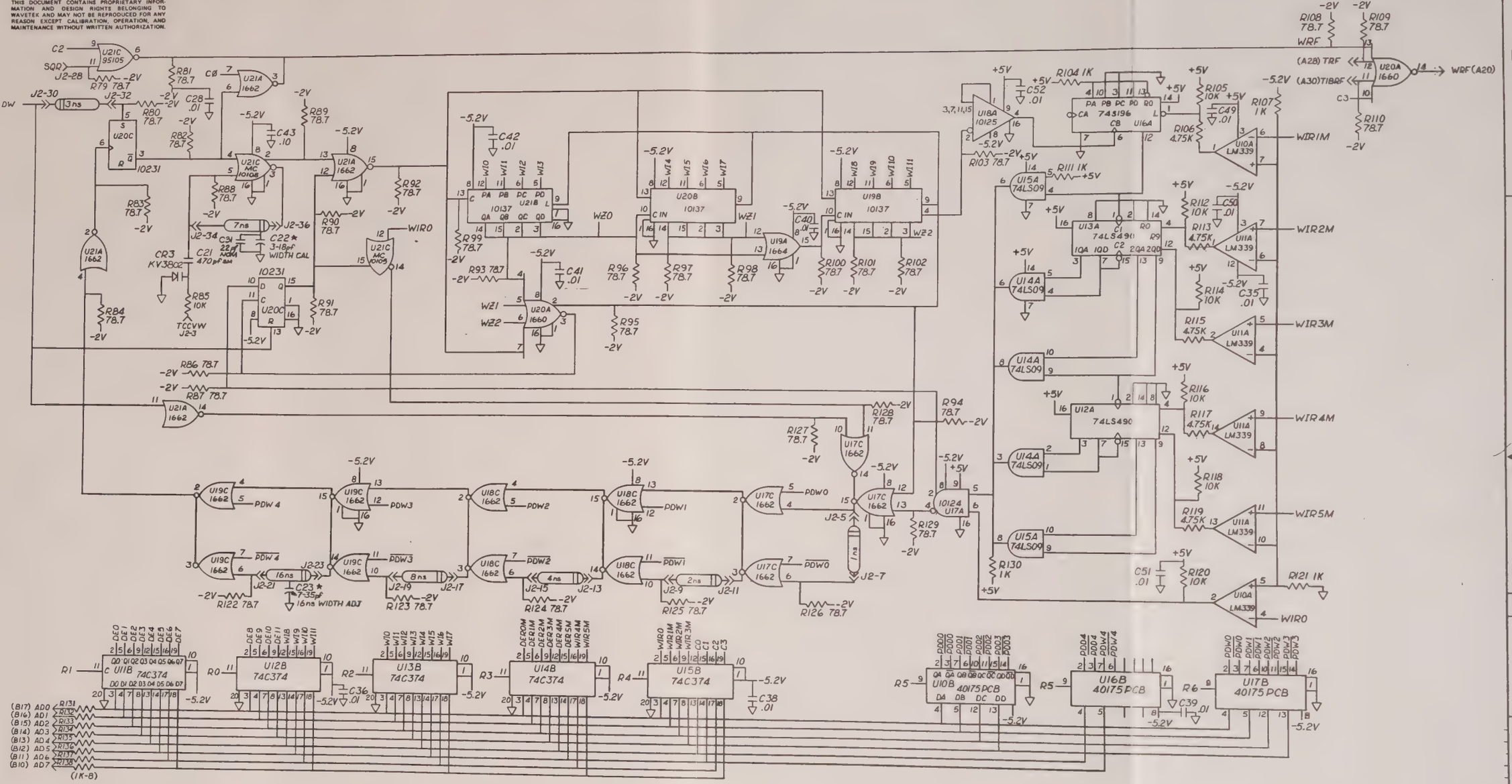
TITLE: TRIGGER/BURST ASSEMBLY

MODEL NO: 859-S-902 | DWG NO: 1100-00-1262 | REV

CODE IDENT: 23338 | SHEET 1 OF 1


THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION
DELAY PIGGY BACK BD.
P/N 1208-00-0697
25°C ZERO BAL
WIDTH ADJ 4V
+50°C CAL WIDTH
4V ADJ DELAY
50°C DELAY CAL
TSV
TCCVW
TCCVD
SQR
SQR DELAY ADJ
DELAY CAL
CV CH2ID
DERIT
DER2T
DER3T
DER4T
DER5T
DER1M
DER2M
DER3M
DER4M
DER5M
DEROM
PDD4
PDD3
PDD2
PDD1
PDD0
DELAY ADJ
(A/B45)
(A/B50)
(A/B 37,38)
(A/B 40,41)
(A/B 43)
(A/B 19,21,23,32, 33,34,35) D6
(B 25,27,29,31,20)
(A24)
(A26) ODLY
(B6) AA2
(B5) AA3
(B3) AA4
(B8) AA0
(B7) AA1
(B4) STRBI
5. THESE COMPONENTS MARKED ★ ARE LOCATED ON 1208-00-0697 SUB-SUB ASSY.
4. PARTIAL REFERENCE DESIGNATIONS SHOWN PREFIX WITH ASSY REF DES (A8).
3. ALL RESISTOR VALUES ARE OHMS
2. ALL CAPACITOR VALUES ARE μf
1. ALL RESISTORS ARE 78.7 Ω, 1/8 W, CC
NOTE: UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. CHERMACK
DATE 1-20-82
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC: DELAY & WIDTH CKTS (A8)
MODEL NO 859-5-902
DWG NO 0103-00-1260
REV
CODE IDENT 23338
SHEET 1 OF 2
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3004

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

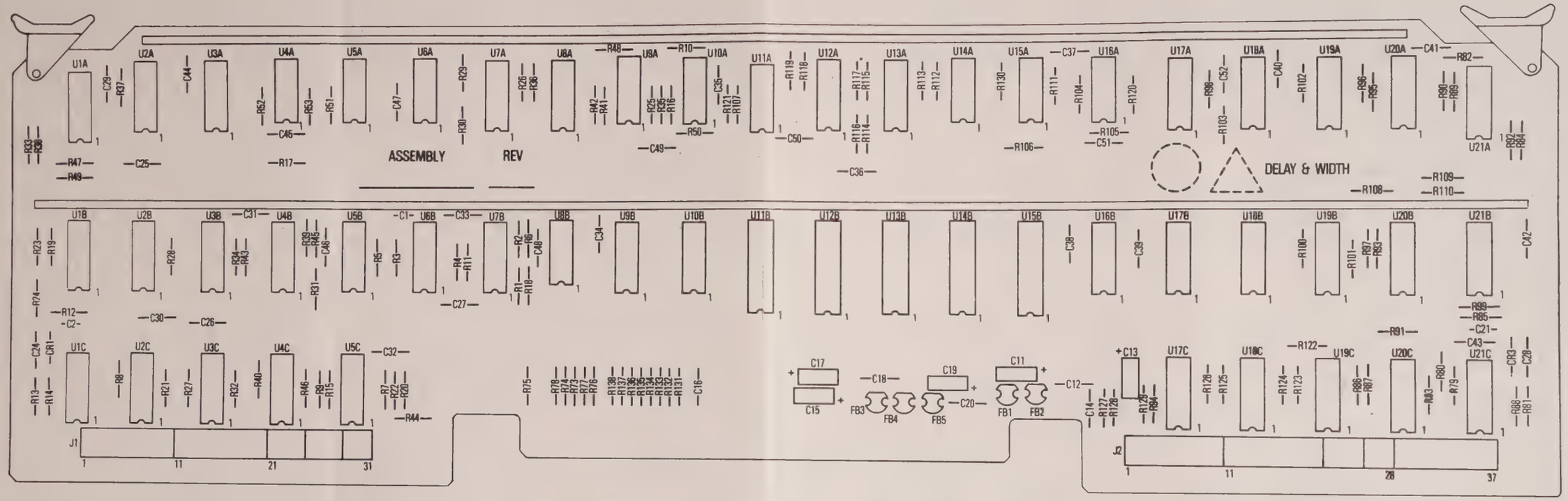


NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 1-1966	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: DELAY & WIDTH CKTS
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO [illegible]	DWG NO 0103-00-126C REV
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: DELAY & WIDTH
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX		
	DO NOT SCALE DWG		MODEL NO: 859
	SCALE		DWG NO: 1100-00-1260 REV
			CODE IDENT: 23338 SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFOR MATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. DELAY/WID	0101-00-1260	WVTK	0101-00-1260	1
NONE	SCHEMATIC. DELAY/WID	0103-00-1260	WVTK	0103-00-1260	1
NONE	PCA, DELAY PIGGY'BK	859-0697	WVTK	1208-00-0697	1
C12 C14 C16 C18 C20 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52	CAP, CER, MN, .01MF, 50V	CACD2Z5U103Z100A	CORNG	1500-01-0310	34
C1	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C2 C21	CAP, MICA, 470PF, 500V	DM15-471J	ARCO	1500-14-7100	2
C11 C13 C15 C17 C19	CAP, TANT, 10MF, 20V	150D106X9020B2	SPRAG	1500-71-0601	5
NONE	DELAY/WIDTH	859-0694	WVTK	1700-00-0694	1
NONE	CONN	22-17-2042	MOLEX	2100-02-0065	3
NONE	CONN	22-17-2032	MOLEX	2100-02-0066	2
NONE	CONN PC	22-17-2102	MOLEX	2100-02-0089	5
NONE	PC BD EJECTOR	103 BLUE	CALMK	2800-07-0014	2
FB1 FB2 FB3 FB4 FB5	BALUN CORE	2873000902	FARIT	3100-00-0002	5
R5	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	1
R10 R104 R107 R111	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	24

WAVETEK PARTS LIST | TITLE: ASSY, DELAY, WIDTH CIRCUIT PCB | ASSEMBLY NO. 1100-00-1260 | PAGE: 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U10A U11A U9A	IC	MLM339P	MOT	7000-03-3900	3
U4B	IC	HD10136	HIT	7001-01-3600	1
U1A U20A	IC	MC1660	MOT	8000-16-6000	2
U17C U18C U19C U1B U21A U2C U3C U4C U7B	IC	MC1662	MOT	8000-16-6200	9
U19A U2A	IC	MC1664	MOT	8000-16-6400	2
U8B	IC	CD4093BE	RCA	8000-40-9300	1
U16B U9B	IC	F4555B	FAIR	8000-45-5500	2
U14A U15A U5A U6A	IC	74LS09	TI	8000-74-0910	4
U1C U21C	IC	MC10105	MOT	8001-01-0500	2
U17A U5B	IC	MC10124P	MOT	8001-01-2400	2
U18A U3A	IC	MC10125P	MOT	8001-01-2500	2
U19B U20B U21B U2B U3B	IC	MC10137	MOT	8001-01-3700	5
U20C U5C U6B	IC	MC10231	MOT	8001-02-3100	3
U10B U16B U17B	IC	40175	NAT	8004-01-7500	3
U16A U4A	IC	SN748196J	TI	8007-41-9601	2
U11B U12B U13B U14B	IC	74C374	NAT	8007-43-7430	5

WAVETEK PARTS LIST | TITLE: ASSY, DELAY, WIDTH CIRCUIT PCB | ASSEMBLY NO. 1100-00-1260 | PAGE: 3 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R121 R130 R131 R132 R133 R134 R135 R136 R137 R138 R48 R51 R52 R53 R73 R74 R75 R76 R77 R78					
R105 R112 R114 R116 R118 R12 R120 R17 R26 R30 R36 R42 R50 R85	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	14
R106 R113 R115 R117 R119 R16 R25 R29 R35 R41	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	10
R1 R100 R101 R102 R103 R108 R109 R11 R110 R122 R123 R124 R125 R126 R127 R128 R129 R13 R14 R15 R19 R2 R20 R21 R22 R23 R24 R27 R28 R3 R31 R32 R33 R34 R37 R38 R39 R4 R40 R43 R44 R45 R46 R47 R49 R6 R7 R79 R8 R80 R81 R82 R83 R84 R86 R87 R88 R89 R9 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	69
CR1 CR3	DIODE	KV3902	KSW	4803-02-3802	2
NONE	POWER BUSS BAR (LG)	6009-90-0004	WVTK	6009-90-0004	1
NONE	POWER BUS BAR	6009-90-0007	WVTK	6009-90-0007	1

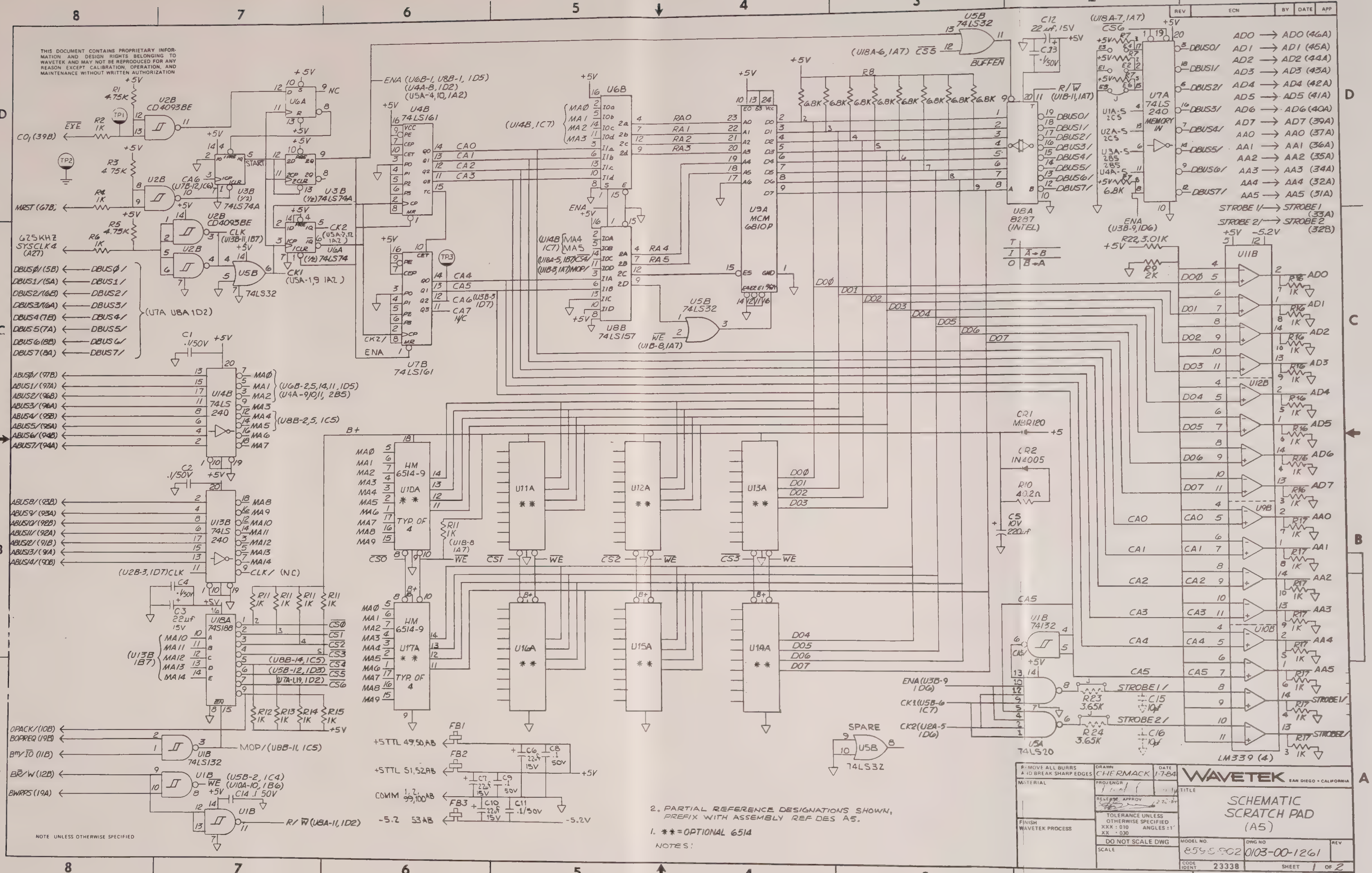
WAVETEK PARTS LIST | TITLE: ASSY, DELAY, WIDTH CIRCUIT PCB | ASSEMBLY NO. 1100-00-1260 | PAGE 2 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U15B					
U12A U13A U7A U8A	IC	74LS490	TI	8007-44-9010	4

WAVETEK PARTS LIST | TITLE: ASSY, DELAY, WIDTH CIRCUIT PCB | ASSEMBLY NO. 1100-00-1260 | PAGE 4 | REV

NOTE UNLESS OTHERWISE SPECIFIED

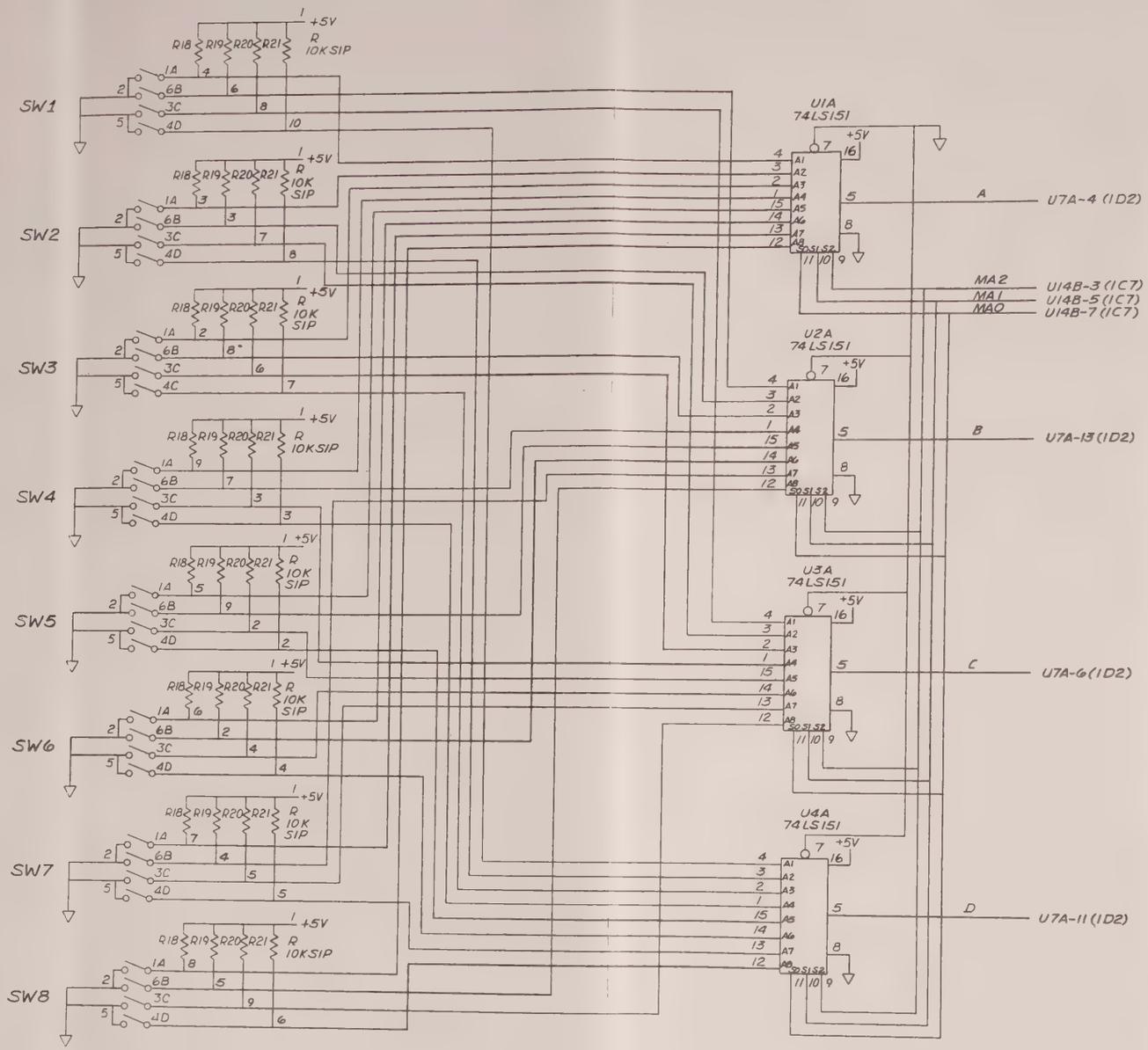
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: DELAY/WIDTH ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 859-S-902 DWG NO. 1100-00-1260 REV
	SCALE		CAGE NO. 23338 SHEET 1 OF 1



THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION
U2B CD4093BE
U6A
U4B 74LS161
U3B (1/2) 74LS74A
U5B 74LS32
U7B 74LS161
U6B
U8B 74LS157
U9A MCM 6810P
U8A 8287 (INTEL)
U7A 74LS 240 MEMORY IN
U14B 74LS 240
U13B 74LS 240
U18A 74S188
U1B 74LS132
U1DA HM 6514-9 TYP. OF 4
U17A HM 6514-9 TYP. OF 4
U11A
U12A
U13A
U16A
U15A
U14A
U5A 74LS20
U1B 74132
LM339 (4)
SPARE U5B 74LS32
CR1 MBR120
CR2 IN4005
R10 40.2Ω
C5 10V 220uf
R22, 3.01K
R9 2K
625KHZ SYSCLK4 (A27)
MRST (67B)
CO1 (39B)
OPACK/(10B)
BOPREQ (19B)
BR/W (12B)
BWRPS (19A)
R/W (U8A-11, 1D2)
MOP/(U8B-11, 1C5)
+5TTL 49,50,AB
+5TTL 51,52AB
COMM 1,2, 99,100AB
-5.2 53AB
STROBE 1/ → STROBE 1 (33A)
STROBE 2/ → STROBE 2 (32B)
2. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REF DES A5.
1. ✱✱=OPTIONAL 6514
NOTES:
NOTE UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN CHERMACK
DATE 1-7-84
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 XX : 030 ANGLES ±1°
DO NOT SCALE DWG
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC SCRATCH PAD (A5)
MODEL NO. 8595-902
DWG NO 0103-00-1261
CODE IDENT 23338
SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

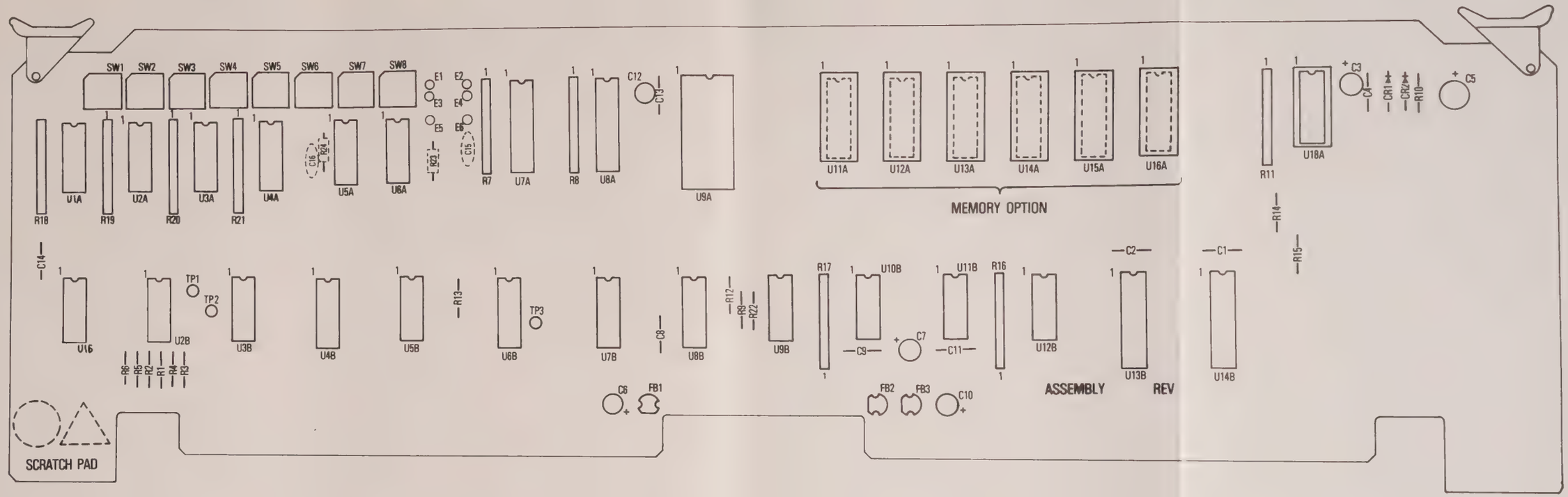


NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: CHERMACK	DATE: 12-6-79	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC SCRATCH PAD
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010, XX ± .030, ANGLES ± 1		
	DO NOT SCALE DWG	MODEL NO: [illegible]	DWG NO: 0103-00-1261 REV
	SCALE	CODE IDENT: 23338	SHEET 2 OF 2

B SHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3284

THIS DOCUMENT CONTAINS PROPRIETARY INFOR
MATION AND DESIGN RIGHTS BELONGING TO
WAVETEK AND MAY NOT BE REPRODUCED FOR ANY
REASON EXCEPT CALIBRATION, OPERATION AND
MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCRATCH PAD RAM
	MFG ENGR		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES 1° .XX .030		
	DO NOT SCALE DWG		MODEL NO 859
	SCALE		DWG NO 1100-00-1261 REV
			CODE IDENT 23338 SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, SCRATCH PAD	0101-00-1261	WVTK	0101-00-1261	1
NONE	SCHEMATIC, SCRATCH PAD	0103-00-1261	WVTK	0103-00-1261	1
C1 C11 C13 C14 C2 C4 C8 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	8
C10 C12 C3 C6 C7	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	5
C5	CAP, TANT, 220MF, 10V	196D227X9010TE4	SPRAG	1500-72-2701	1
NONE	SCRATCH PAD	859-0688	WVTK	1700-00-0688	1
NONE	SKT, IC, 18 PIN	18-DIP	CINCH	2100-03-0023	6
NONE	SKT, IC, 16PIN	DILB-16P-108	BURND	2100-03-0028	1
TP1 TP2 TP3	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	3
4	PC BD EJECTOR	103 WHITE	CALMK	2800-07-0008	2
FB1 FB2 FB3	BALUN CORE	2673000902	FARIT	3100-00-0002	3
R12 R13 R14 R15 R2 R4 R6	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	7
R9	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	1
R22	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	1
R10	RES, MF, 1/8W, 1%, 40.2	RN55D-40R2F	TRW	4701-03-4029	1
R1 R3 R5	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	3

WAVETEK PARTS LIST | TITLE ASSY, SCRATCH PAD BOARD | ASSEMBLY NO 1100-00-1261 | PAGE 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R18 R19 R20 R21	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	4
R7 R8	RES MODULE	4310R-101-682	BOURN	4770-00-0016	2
R11 R16 R17	RES MODULE	4310R-101-102	BOURN	4770-00-0022	3
CR2	DIODE	1N4005	MOT	4806-01-4005	1
CR1	DIODE	MBR 120	MOT	4806-02-0120	1
SW1 SW2 SW3 SW4 SW5 SW6 SW7 SW8	SWITCH, PC ROTARY	2300029	EECO	5107-00-0007	8
U10B U11B U12B U9B	IC	MLM339P	MOT	7000-03-3900	4
U2B	IC	CD4093BE	RCA	8000-40-9300	1
U9A	IC	MLM6810AL	MOT	8000-68-1000	1
U5A	IC	74LS20	TI	8000-74-2010	1
U5B	IC	74LS32	TI	8000-74-3210	1
U3B U6A	IC	74LS74	TI	8000-74-7410	2
U6A	IC	DP8303	NAT	8000-83-0300	1
U1B	IC	74132	TI	8007-41-3200	1
U1A U2A U3A U4A	IC	74LS151	TI	8007-41-5110	4
U6B U8B	IC	74LS157	TI	8007-41-5710	2
U4B U7B	IC	74LS161	SIG	8007-41-6110	2

WAVETEK PARTS LIST | TITLE ASSY, SCRATCH PAD BOARD | ASSEMBLY NO. 1100-00-1261 | PAGE 2 | REV

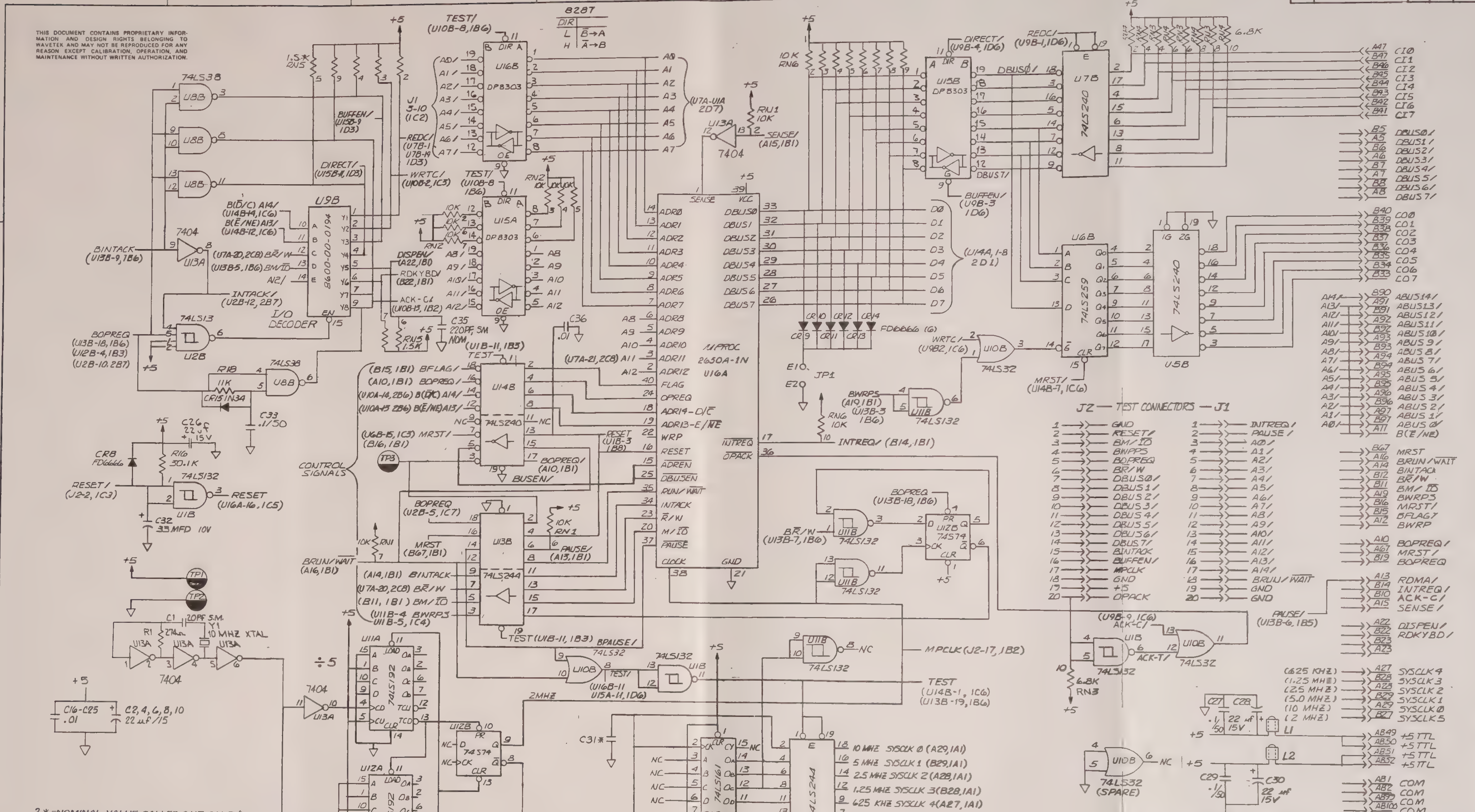
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U13B U14B U7A	IC	74LS240	TI	8007-42-4010	3
U18A	IC, PROGRAMMED REF 8007-41-8801	8600-00-0190	WVTK	8600-00-0190	1

WAVETEK PARTS LIST | TITLE ASSY, SCRATCH PAD BOARD | ASSEMBLY NO 1100-00-1261 | PAGE 3 | REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: SCRATCH PAD ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 859-S-902 / DWG NO 1100-00-1261 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



74LS38
U8B
U9B
8600-00-0194
I/O DECODER
7404
U13A
BINTACK (U13B-9,1B6)
74LS13
U2B
BOPREQ (U13B-18,1B6) (U12B-4,1B3) (U2B-10,2B7)
INTACK/ (U2B-12,2B7)
R18 11K
CR15 1N34
C33 .1/50
CR8 FD6666
R16 30.1K
74LS132
U1B
RESET/ (J2-2,1C3)
RESET (U16A-16,1C5)
C32 33MFD 10V
C26 22 uf 15V
TP1
TP2
TP3
C1 20PF S.M.
Y1 10 MHZ XTAL
R1 274Ω
C16-C25 .01
C2,4,6,8,10 22 uf/15
1.5K* RN5
BUFFEN/ (U15B-9 1D3)
DIRECT/ (U15B-11,1D3)
J1 3-10 (1C2)
REDC/ (U7B-1 U7B-19 1D3)
WRTC/ (U10B-2,1C3)
DISPEN/ (A22,1B0)
RDKYBD/ (B22,1B1)
ACK-C/ (U10B-13,1B2)
C35 220PF, SM NOM
TEST/ (U10B-8,1B6)
U16B DP8303
U15A DP8303
RN2 10K
8287
DIR L B→A H A→B
(U7A-U1A 2D7)
RN1 10K
SENSE/ (A15,1B1)
U16A 2650A-1N
μPROC
C36 .01
CONTROL SIGNALS
U14B 74LS240
BUSEN/
BOPREQ/ (A10,1B1)
U13B 74LS244
PAUSE/ (A13,1B1)
BRUN/WAIT (A16,1B1)
TEST (U1B-11,1B3)
BPAUSE/
74LS32
U10B
TEST/ (U16B-11 U15A-11,1D6)
÷5
U11A 74LS192
U12A 74LS192
U12B 74S74
10MHZ
2MHZ
2MHZ/
C31*
U3B 74LS161
U4B 74LS244
10 MHZ SYSCLK 0 (A29,1A1)
5 MHZ SYSCLK 1 (B29,1A1)
2.5 MHZ SYSCLK 2 (A28,1A1)
1.25 MHZ SYSCLK 3 (B28,1A1)
625 KHZ SYSCLK 4 (A27,1A1)
2MHZ SYSCLK 5 (B27,1A1)
BWRP (A12,1B1)
WRP (U16A-22,1B5)
CLOCK GENERATOR
MPCLK (J2-17,1B2)
TEST (U14B-1,1C6) (U13B-19,1B6)
INTREQ/ (B14,1B1)
FD6666 (6)
JP1
RN6 10K
U11B 74LS132
BWRPS (A19,1B1)
U15B DP8303
U7B 74LS240
6.8K
U6B 74LS259
U5B 74LS240
MRST/ (U14B-7,1C6)
CI0 CI1 CI2 CI3 CI4 CI5 CI6 CI7
DBUS0/ DBUS1/ DBUS2/ DBUS3/ DBUS4/ DBUS5/ DBUS6/ DBUS7/
CO0 CO1 CO2 CO3 CO4 CO5 CO6 CO7
ABUS14/ ABUS13/ ABUS12/ ABUS11/ ABUS10/ ABUS 9/ ABUS 8/ ABUS 7/ ABUS 6/ ABUS 5/ ABUS 4/ ABUS 3/ ABUS 2/ ABUS 1/ ABUS 0/
B(E/NE)
MRST
BRUN/WAIT
BINTACK
BR/W
BM/IO
BWRPS
MRST/
BFLAG/
BWRP
BOPREQ/
MRST/
BOPREQ
RDMA/
INTREQ/
ACK-C/
SENSE/
DISPEN/
RDKYBD/
SYSCLK4 SYSCLK3 SYSCLK2 SYSCLK1 SYSCLK0 SYSCLK5
+5 TTL
COM
J2 — TEST CONNECTORS — J1
1 GND 2 RESET/ 3 BM/IO 4 BWPPS 5 BOPREQ 6 BR/W 7 DBUS0/ 8 DBUS1/ 9 DBUS2/ 10 DBUS3/ 11 DBUS4/ 12 DBUS5/ 13 DBUS6/ 14 DBUS7/ 15 BINTACK 16 BUFFEN/ 17 MPCLK 18 GND 19 +5 20 OPACK
1 INTREQ/ 2 PAUSE/ 3 A0/ 4 A1/ 5 A2/ 6 A3/ 7 A4/ 8 A5/ 9 A6/ 10 A7/ 11 A8/ 12 A9/ 13 A10/ 14 A11/ 15 A12/ 16 A13/ 17 A14/ 18 BRUN/WAIT 19 GND 20 GND
ACK-T/
6.8K RN3
74LS32 (SPARE)
C27 C28 .1/50 22 uf 15V
L1 L2
C29 .1/50
C30 22 uf 15V

2.* =NOMINAL VALUE CALLED OUT ON P/L.

1. I.C. POWER SUPPLY FOR:
 14 PIN DIP= PIN 7, GND; PIN 14, +5
 16 PIN DIP= PIN 8, GND; PIN 16, +5
 18 PIN DIP= PIN 9, GND; PIN 18, +5
 20 PIN DIP= PIN 10, GND; PIN 20, +5
 24 PIN DIP= PIN 12, GND; PIN 24, +5

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 12-1-83
MATERIAL	PROJ ENGR	
FINISH WAVETEK PROCESS	RELEASE APPROV	12-20-84
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030	
	DO NOT SCALE DWG	
	SCALE NONE	

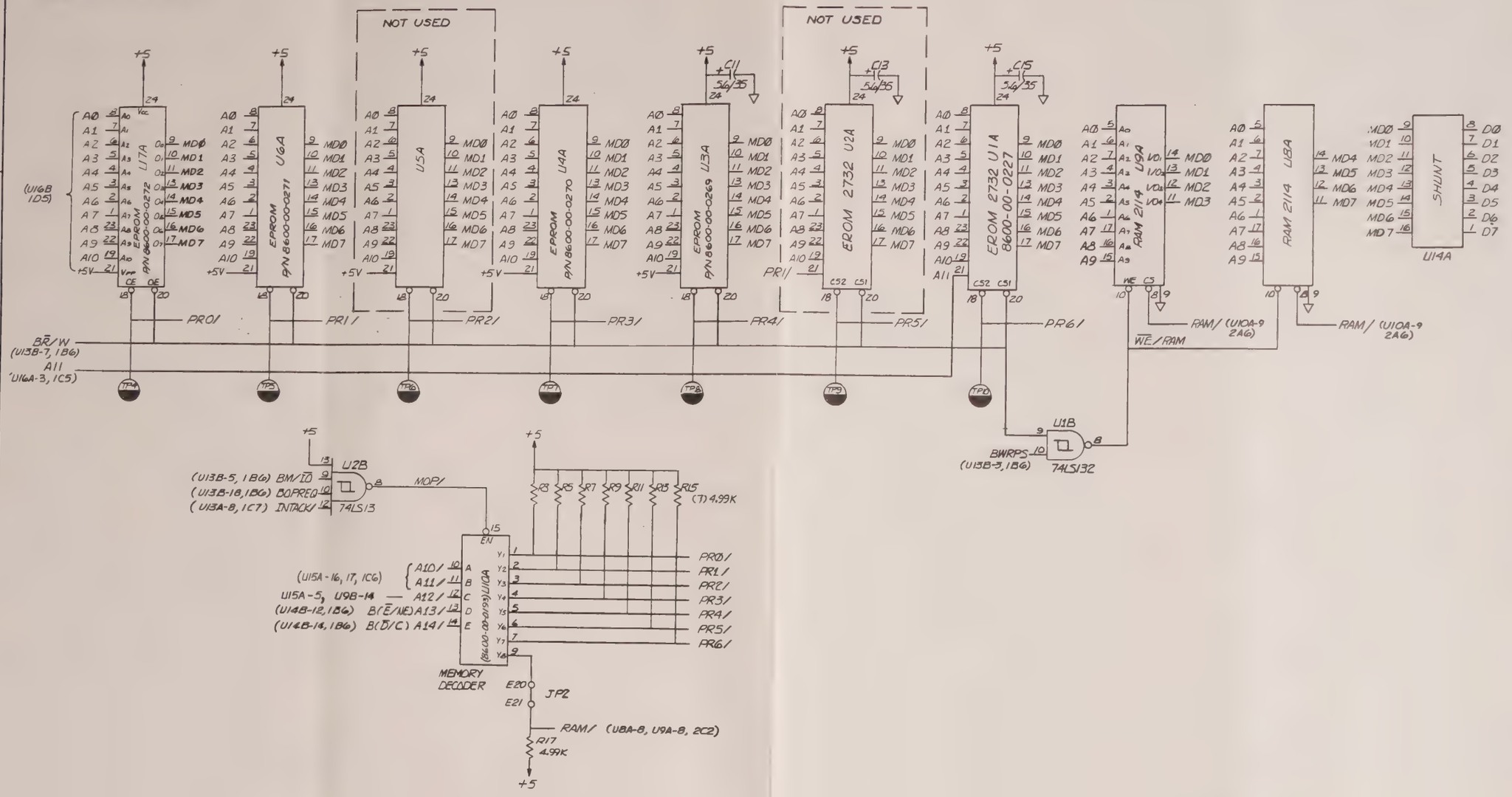
WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC - MICRO PROCESSOR

MODEL NO	DWG NO.	REV
859-5-32	0103-00-1263	
CODE IDENT 23338	SHEET 1 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

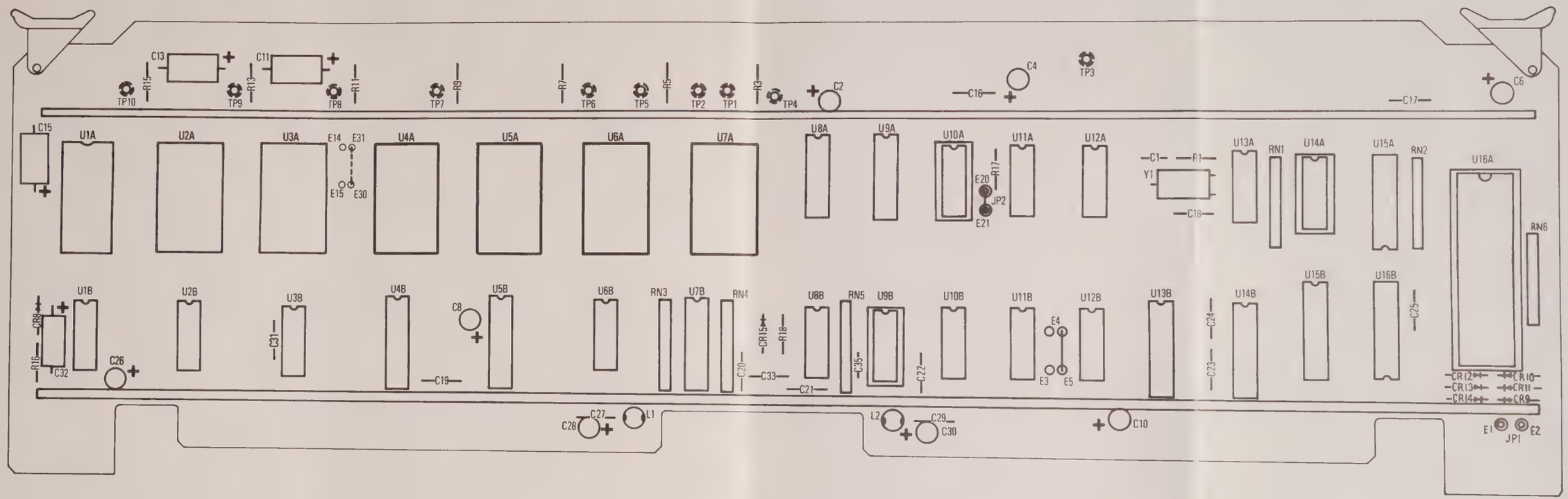
REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 12-1-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE: SCHEMATIC - MICRO PROCESSOR (EPROM MEMORY)
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859-5-902	DWG NO 0103-00-1263 REV
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROTOTYPE		TITLE: MICROPROCESSOR
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES 1° .XX .030		
	DO NOT SCALE DWG		MODEL NO: 859
	SCALE		DWG NO: 1100-00-1263 REV
			COMPANY 23338 SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, M-PROC	0101-00-1263	WVTK	0101-00-1263	1
NONE	SCHEMATIC, M-PROC	0103-00-1263	WVTK	0103-00-1263	1
C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C36	CAP, CER, MN, .01MF, 50V	CACD?Z5U103Z100A	CORNG	1500-01-0310	11
C27 C29 C33	CAP, CER, MON, .1MF, 50V	CACD?Z5U104Z050A	CORNG	1500-01-0405	3
C31T	CAP, CER, 56PF, 1KV	DD-560	CRL	1500-05-6001	1
C1	CAP, MICA, 20PF, 500V	DM15-200J	ARCO	1500-12-0000	1
C35T	CAP, MICA, 220PF, 500V	DM15-221J	ARCO	1500-12-2100	1
C10 C2 C26 C28 C30 C4 C6 C8	CAP, TANT, 22MF, 15V	196D?26X9015KA1	SPRAG	1500-72-2601	8
C32	CAP, TANT, 33MF, 10V	150D?36X9010B2	SPRAG	1500-73-3601	1
C11 C13 C15	CAP, TANT, 5.6MF, 35V	150D?65X9035B2	SPRAG	1500-75-6302	3
NONE	M-PROC	859-?699	WVTK	1700-00-0699	1
NONE	SKT, IC, 16PIN	DILB-16P-108	BURND	2100-03-0028	3
NONE	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	7
NONE	SKT, IC, 40PIN	DILB-40P-108	BURND	2100-03-0030	1
Y1	CRYSTAL, 10MHZ	590-?02	WVTK	2300-99-0006	1
NONE	PC BD EJECTOR	103 ?HITE	CALMK	2800-07-0008	2

WAVETEK PARTS LIST | TITLE: ASSY, MICROPROCESSOR BOARD | ASSEMBLY NO. 1100-00-1263 | PAGE: 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	TRANSIPAD	10123N	METRS	2800-11-0003	2
1	SHUNT	435704-8	AMP	3000-00-0033	1
NONE	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	1
NONE	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	4
L1 L2	BALUN CORE	2873000902	FARIT	3100-00-0002	2
R18	RES, MF, 1/8W, 1%, 11K	RN55D-1102F	TRW	4701-03-1102	1
R1	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R16	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R11 R13 R15 R17 R3 R5 R7 R9	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	8
RN1 RN2 RN6	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	3
RN5	RES NETWK	785-?R1.5K	BECK	4770-00-0010	1
RN3 RN4	RES MODULE	4310R-101-682	BOURN	4770-00-0016	2
CR15	DIODE	1N34	FAIR	4804-01-0034	1
CR10 CR11 CR12 CR13 CR14 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	7
NONE	POWER BUSS BAR (LG)	6009-90-0004	WVTK	6009-90-0004	2
U8A U9A	IC	2114	INTEL	8000-21-1400	2

WAVETEK PARTS LIST | TITLE: ASSY, MICROPROCESSOR BOARD | ASSEMBLY NO. 1100-00-1263 | PAGE: 2 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U16A	IC	SCN2650AC2N40	SIG	8000-26-5001	1
U13A	IC	7404	TI	8000-74-0400	1
U2B	IC	SN74LS13N	TI	8000-74-1310	1
U10B	IC	74LS32	TI	8000-74-3210	1
U8B	IC	74LS38	TI	8000-74-3810	1
U12B	IC	74S74	TI	8000-74-7401	1
U15A U15B U16B	IC	DP8303	NAT	8000-83-0300	3
U11B U1B	IC	74LS132	TI	8007-41-3210	2
U3B	IC	74LS161	SIG	8007-41-6110	1
U11A U12A	IC	74LS192	TI	8007-41-9210	2
U14B U5B U7B	IC	74LS240	TI	8007-42-4010	3
U13B U4B	IC	74LS244	TI	8007-42-4410	2
U6B	IC	SN74LS259N	TI	8007-42-5910	1
U10A	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0193	WVTK	8600-00-0193	1
U9B	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0194	WVTK	8600-00-0194	1
U1A	IC, PROGRAMMED	8600-00-0227	WVTK	8600-00-0227	1

WAVETEK PARTS LIST | TITLE: ASSY, MICROPROCESSOR BOARD | ASSEMBLY NO. 1100-00-1263 | PAGE: 3 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	FROM 8000-27-3200				
U3A	IC, PROGRAMMED REF. 8000-27-1600	8600-00-0269	WVTK	8600-00-0269	1
U4A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0270	WVTK	8600-00-0270	1
U6A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0271	WVTK	8600-00-0271	1
U7A	IC, PROGRAMMED REF 8000-27-1600	8600-00-0272	WVTK	8600-00-0272	1

WAVETEK PARTS LIST | TITLE: ASSY, MICROPROCESSOR BOARD | ASSEMBLY NO. 1100-00-1263 | PAGE 4 | REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: MICROPROCESSOR BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		
	SCALE		859-S-902 / DWG NO 1100-00-1263 / REV
			CAGE 23338 / SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PROM INSTALLATION DRAWING	0109-00-0018	WVTK	0109-00-0018	1
U3A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0195	WVTK	8600-00-0195	1
U7A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0198	WVTK	8600-00-0198	1
U4A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0251	WVTK	8600-00-0251	1
U6A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0252	WVTK	8600-00-0252	1

WAVETEK PARTS LIST

TITLE
PROM PACKAGE
MICRO-PROC
1100-00-0699

ASSEMBLY NO.
1109-00-0018

PAGE: 1

REV
A

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN | DATE

PROJ ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ±1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
MICRO-PROC PROM PACKAGE

MODEL NO. 859-S-902

DWG NO. 1109-00-0018

REV A

CODE IDENT 23338

SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO. 42708

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SPECIFICATION DRWG	859-1322	WVTK	0108-00-1322	1
NONE	INSTALLATION DRAWING	0109-00-1322	WVTK	0109-00-1322	1
U11B	IC REF: 1205-00-1322 SPEC SHEET	100102 DTD >2-4-83	FAIR	8100-00-0008	1
U5A	IC, PROGRAMMED REF: 8007-44-7101	8600-00-0274	WVTK	8600-00-0274	1

WAVETEK PARTS LIST	TITLE ASSY, SELECTED SET OF IC'S	ASSEMBLY NO. 1205-00-1322 PAGE: 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SELECTED SET OF IC'S
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 859-S-902	DWG NO. 1205-00-1322 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BUNKER GRAPHICS ACCUPRESS
REORDER NO. 42186

MP MASTER
MA35708